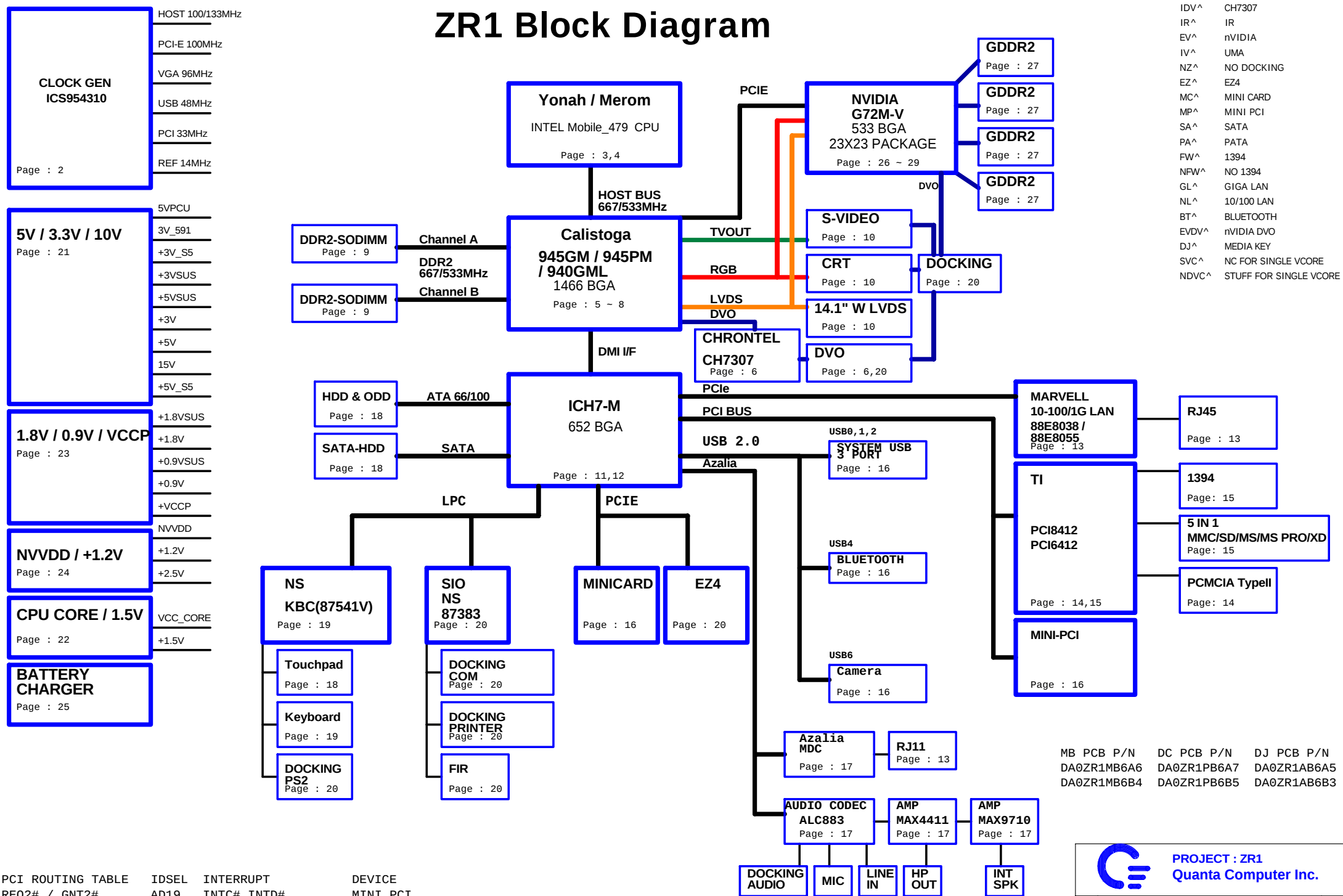


MODEL :		REV:	CHANGE LIST:	ECN NO	MODEL : ZR1 MB		
ZR1 MotherBoard	1A	FIRST RELEASE		E200604-0013 E200605-0194	PAGE	FROM	TO
	2A	PAGE 02 : ADD EMI SOLUTION PAGE 03 : MODIFY MDC NUT / UN-STUFF CPURST# PU R151 PAGE 06 : STUFF LIB R430 FOR 940GML / MOVE TMD5 PU AT NB SIDE PAGE 10 : ADD LCD PIN 31 & 33 TO GND FOR EMI / MODIFY S-VIDEO CONNECTOR P/N PAGE 11 : MODIFY RTC BATTERY CONNECTOR / ADD MB GPIO FOR FACTORY IDENTIFY / REMOVE SUSCLK FOR SMSC SIO PAGE 13 : MODIFY VMAIN AVAL TO +3V S5 / UN-STUFF R28 & R29 FOR LAN LED NO ACTIVE ISSUE PAGE 16 : ADD MINI-CARD BYPASS CAPACITOR BY ACER REQUEST / ALWAYS STUFF D11 FOR MINI-CARD W/L CAN'T ENABLE PAGE 17 : ADD L64 ON SPDIF FOR EMI / MODIFY BEEP NOISE (R281) / ADD C695,C696 FOR REDUCE LINE IN NOISE / MODIFY SPDIF CIRCUIT PAGE 18 : MODIFY R522,R524 FOR REDUCE DISTORTION / RESERVE R541,R542,R543 FOR NOISE REDUCTION / STUFF U41 / UN-STUFF D30 FOR POP ISSUE PAGE 20 : MODIFY SIO TO NS87383 / ADD RGB EMI SOLUTION / RESERVE DVI EMI SOLUTION / UN-STUFF TMD5 PU AT DOCKING SIDE PAGE 21 : MODIFY PL2,PL5 TO 2R5 FOR REDUCE POWER RIPPLE & INCREASE POWER BUDGET PAGE 22 : SOLVE CPU VCORE UN-STABLE ISSUE TO CHANGE SERVAL COMPONENT VALUE PAGE 23 : MODIFY PL8 TO 2R5 FOR COST DOWN / ADD PC16,PC21 FOR PWM STABILITY / UN-STUFF PR21 FOR WRONG PU POWER LEVEL PAGE 24 : MODIFY PR30 FOR NVVDD POWER QUALITY		E200605-3569 E200605-6558	1	1A	
					2	2A	3A
					3	2A	3A
					4	1A	3A
					5	1A	
					6	2A	3A
					7	1A	
					8	1A	3A
	3A	PAGE 02 : MODIFY C509,C503,C491,C498 to 4.7uF PAGE 03 : REMOVE R102 0 ohm PAGE 04 : Modify C187 to 330uF , remove C222 PAGE 06 : MODIFY C605,C590,C609 to 4.7uF / Add EMI solution C705 ~ C708 PAGE 08 : MODIFY L22,L23,Add PC166,C712-C715 for TV noise / Modify C327,C594 to 330uF;C158,C548 to 10uF / remove R449,R451 0 ohm PAGE 09 : Remove C76,C88 / modify C75 to 100uF PAGE 10 : Modify TV filter circuit / modify LCD VCC circuit PAGE 11 : Add media board GPIO pin PAGE 13 : Modify C99,C97,C98,C61,C79 to 4.7uF PAGE 14 : Remove R497,R222 0 ohm / modify C390,C391,C405,C412 to 4.7uF PAGE 15 : Modify C642,C409 to 4.7uF / modify R163,R164,R161,R153 to RN92,RN93 PAGE 16 : Modify R452,R454 to RN91, R389,R392 to RN90 PAGE 17 : Modify C651,C430,C440,C658,C666 to 4.7uF / Modify SPDIF circuit PAGE 18 : Remove R208,R510 for ODD / Remove R459,R106 0 ohm PAGE 20 : Modify SIO clock & strap R303 PAGE 21 : Remove PR110,PR155,PR114,PR106,PR153 0 ohm / Add PC167 for TV noise PAGE 22 : Remove PR149 0 ohm PAGE 23 : Remove PR24 0 ohm PAGE 24 : Remove NVVDD switching voltage circuit / remove PR135,PR100 0 ohm PAGE 25 : Remove PR28 0 ohm			9	1A	3A
					10	2A	3A
					11	2A	3A
					12	1A	
					13	2A	3A
					14	1A	3A
					15	1A	3A
					16	2A	3A
					17	2A	3A
					18	2A	3A
					19	1A	
					20	2A	3A
					21	2A	3A
					22	2A	3A
					23	2A	3A
					24	2A	3A
					25	1A	3A
					26	1A	
					27	1A	
					28	1A	
					29	1A	
 PROJECT : ZR1		APPROVE BY: JIM HSU	DRAWING BY:JACKY CHENG	REV 3A	COVER SHEET 1 OF 1		
		MB ASSY'S P/N : 31ZR1MB0008,16,24,32,41,59,83,91,B4	PROJECT LEADER: JIM HSU	DOCUMENT NO: 204			DATE :2006/06/26

ZR1 Block Diagram



- IDV^ CH7307
- IR^ IR
- EV^ nVIDIA
- IV^ UMA
- NZ^ NO DOCKING
- EZ^ EZ4
- MC^ MINI CARD
- MP^ MINI PCI
- SA^ SATA
- PA^ PATA
- FW^ 1394
- NFW^ NO 1394
- GL^ GIGA LAN
- NL^ 10/100 LAN
- BT^ BLUETOOTH
- EVDV^ nVIDIA DVO
- DJ^ MEDIA KEY
- SVC^ NC FOR SINGLE VCORE
- NDVC^ STUFF FOR SINGLE VCORE

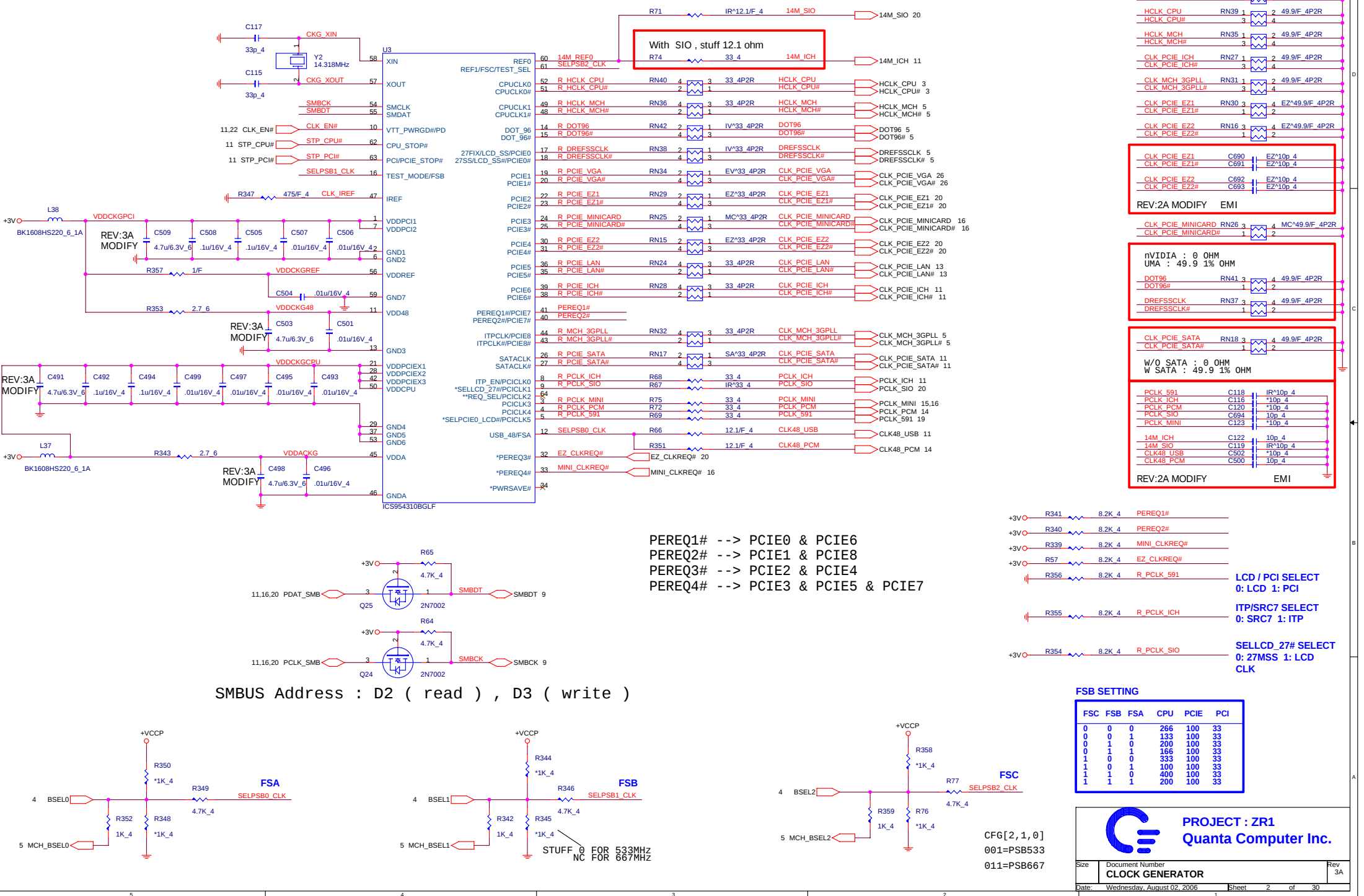
PCI ROUTING TABLE	IDSEL	INTERRUPT	DEVICE
REQ2# / GNT2#	AD19	INTC#, INTD#	MINI PCI
REQ0# / GNT0#	AD25	INTE#, INTF#, INTG#	TI XX12

MB PCB P/N DA0ZR1MB6A6
 DC PCB P/N DA0ZR1PB6A7
 DJ PCB P/N DA0ZR1AB6A5
 DA0ZR1MB6B4 DA0ZR1PB6B5 DA0ZR1AB6B3

PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date: Wednesday, August 02, 2006	Sheet 1 of 30	

CLOCK GENERATOR



PEREQ1# --> PCIE0 & PCIE6
PEREQ2# --> PCIE1 & PCIE8
PEREQ3# --> PCIE2 & PCIE4
PEREQ4# --> PCIE3 & PCIE5 & PCIE7

SMBUS Address : D2 (read) , D3 (write)

FSB SETTING

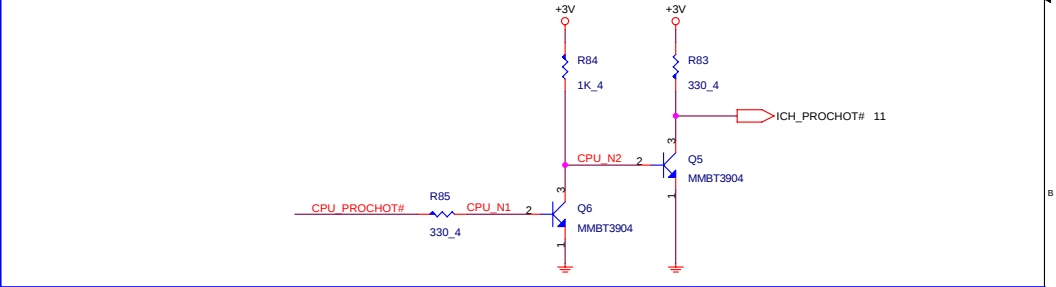
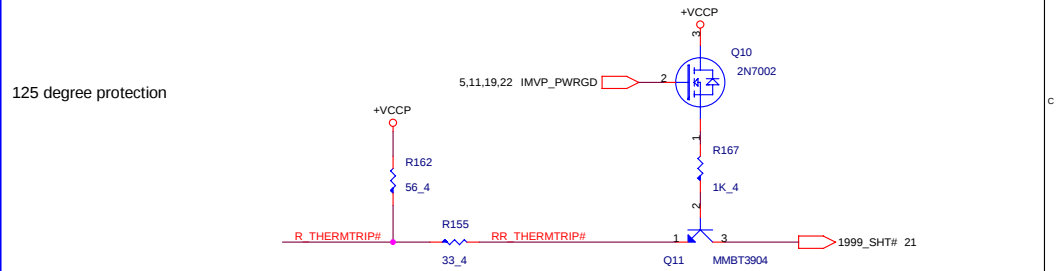
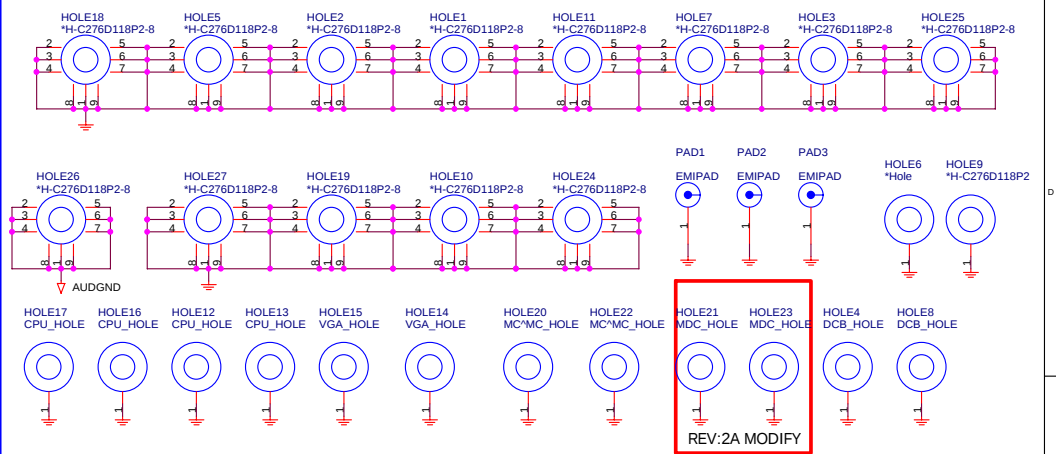
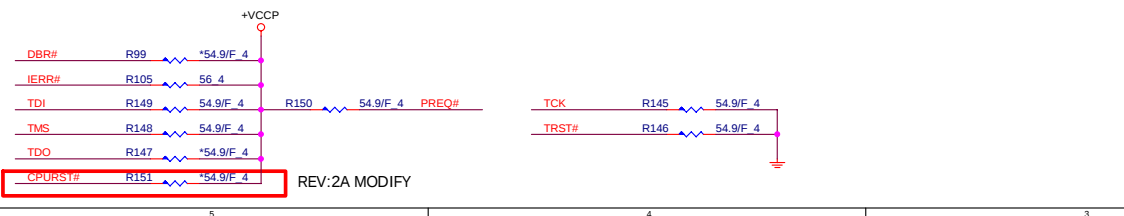
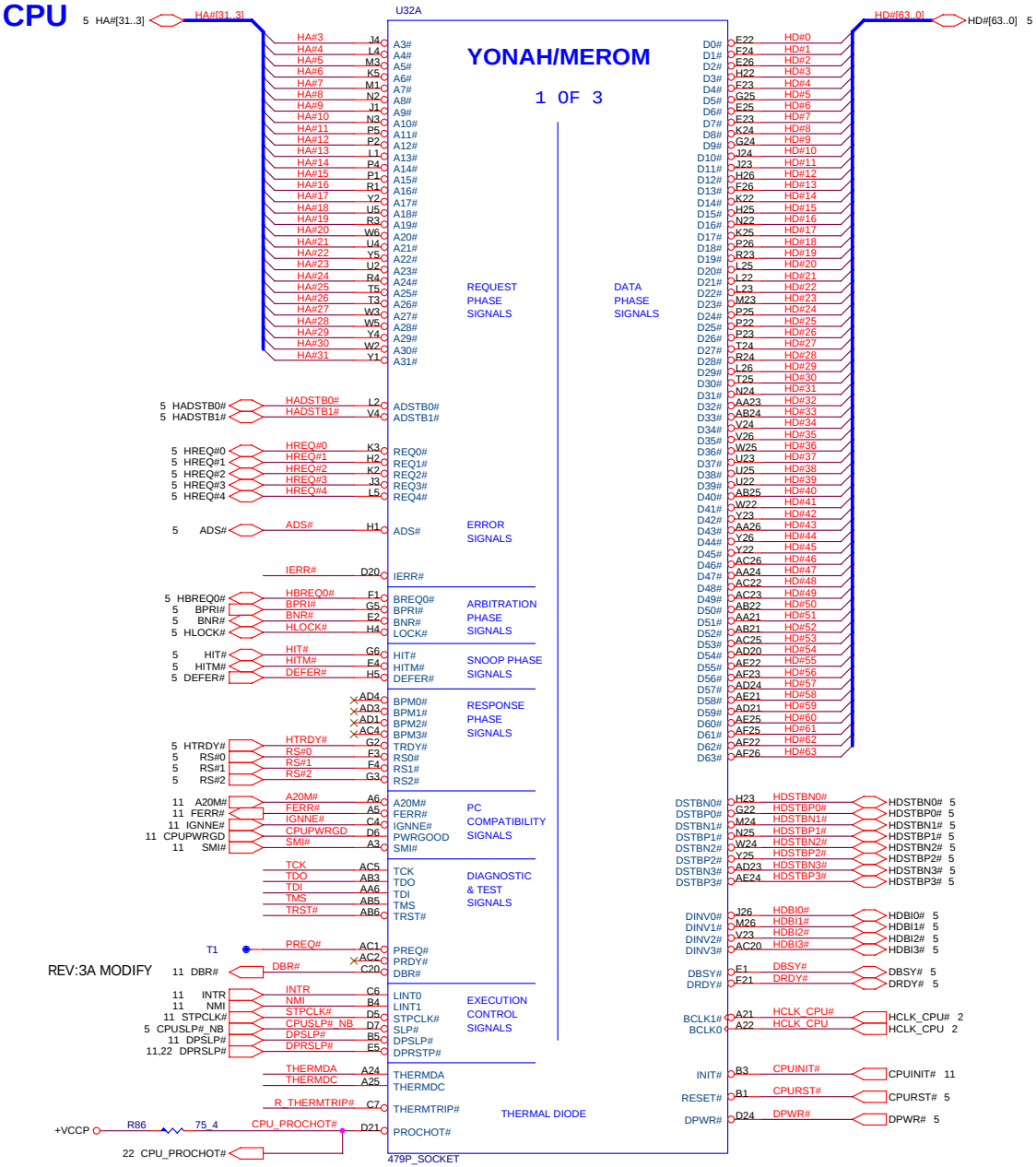
FSC	FSB	FSA	CPU	PCIE	PCI
0	0	0	266	100	33
0	0	1	133	100	33
0	1	0	200	100	33
0	1	1	166	100	33
1	0	0	333	100	33
1	0	1	100	100	33
1	1	0	400	100	33
1	1	1	200	100	33

PROJECT : ZR1
Quanta Computer Inc.

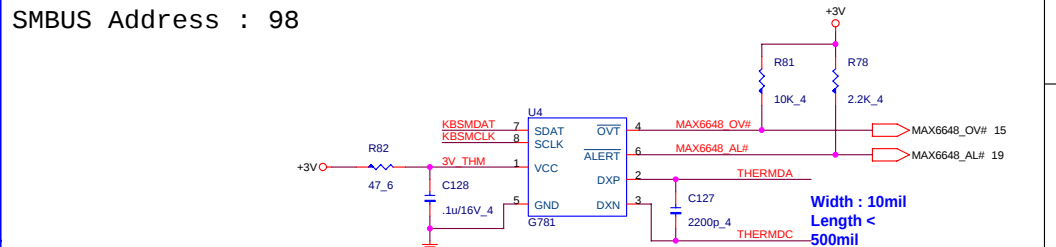
Size Document Number Rev 3A
CLOCK GENERATOR
Date: Wednesday, August 02, 2006 Sheet 2 of 30

CF6[2,1,0]
001=PSB533
011=PSB667

CPU



SMBUS Address : 98



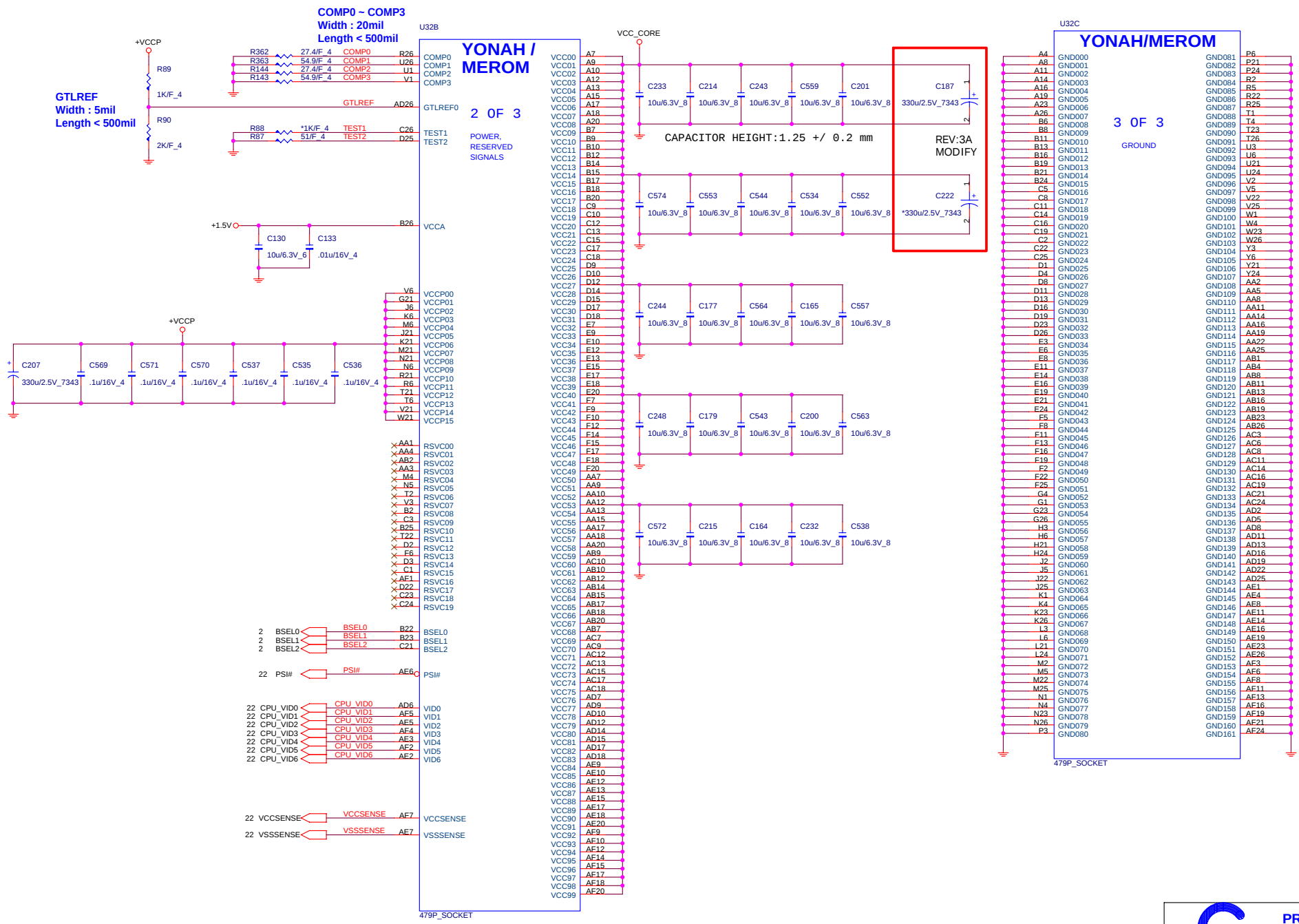
MAXIM 6657 : AL006657020
GMT G781 : AL000781101



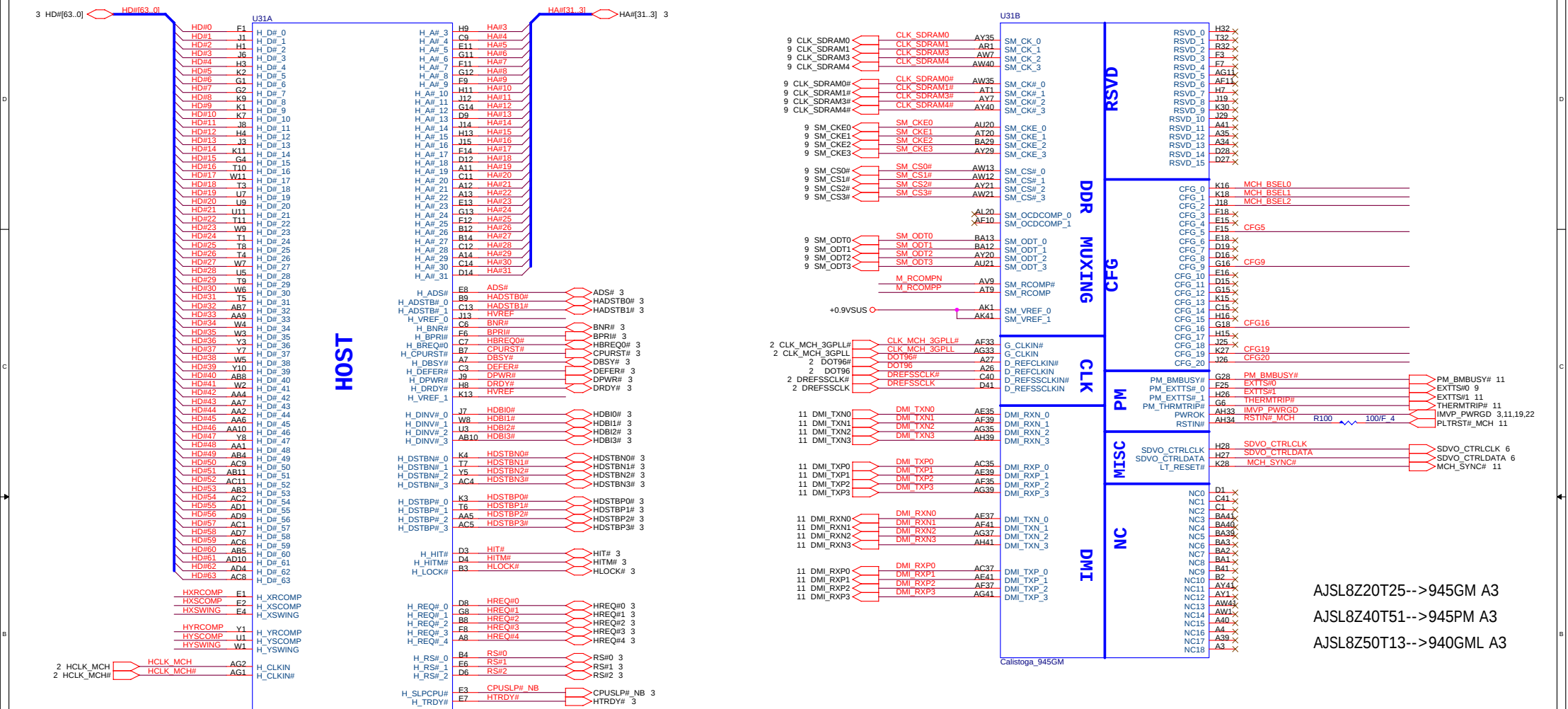
PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number CPU (HOST)	Rev 3A
Date:	Wednesday, August 02, 2006	Sheet 3 of 30

CPU



NB 945GM/PM/940GML



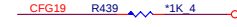
AJSL8Z20T25-->945GM A3

AJSL8Z40T51-->945PM A3

AJSL8Z50T13-->940GML A3

- 1.MCH_CFG_5 : Low = DMI X2, High=DMIX4
- 2.MCH_CFG_6 : Low = Moby Dick, High = Calistoga (Default)
- 3.MCH_CFG_7 : Low = RSVD, High = Mobile CPU
- 4.MCH_CFG_9 PCI Exp Graphics Lane: Low = Reverse lane ,High=Normal
- 5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
- 6.MCH_CFG_11: PSB 4x Enable : Low=Rsvd, High=Calistoga.
- 7.MCH_CFG_16 FSB Dymnic ODT: Low = Dynamic ODT Disabled,
High= Dynamic ODT Enabled.
- 8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
- 9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.
- 10.MCH_CFG_20 PCIE Backward interoperability mode: Low=
only SDVO or PCIE x1 is operational(defaults) ,
High=SDVO and PCIE x1 are operation
simultaneously via the PEG port.

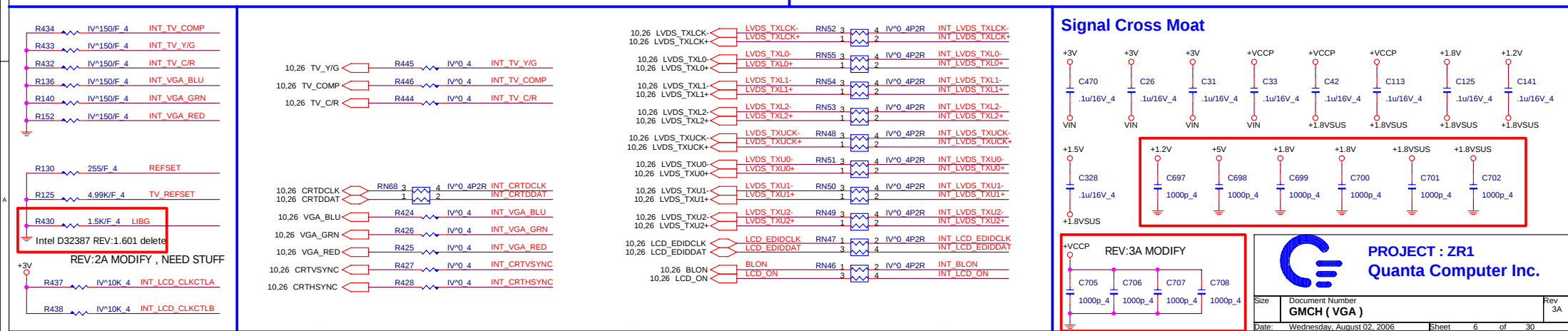
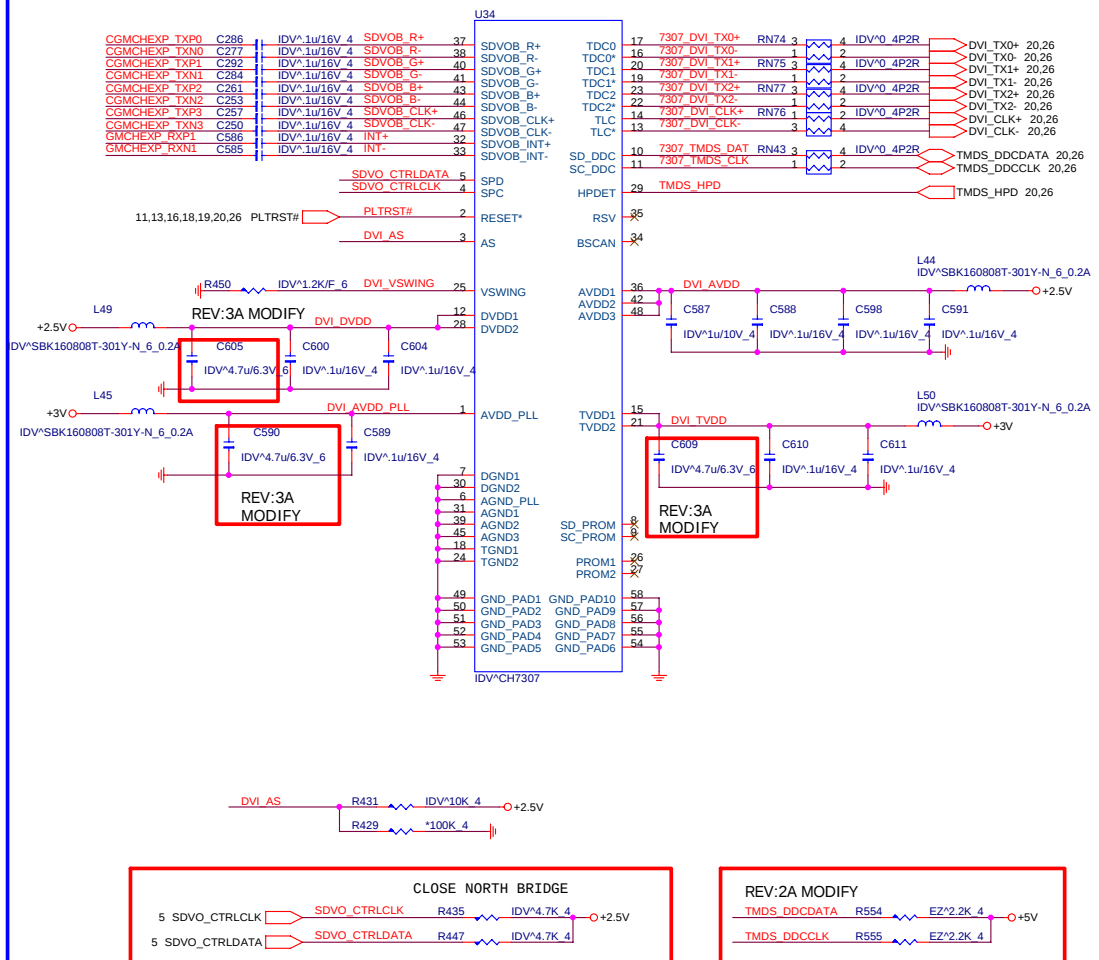
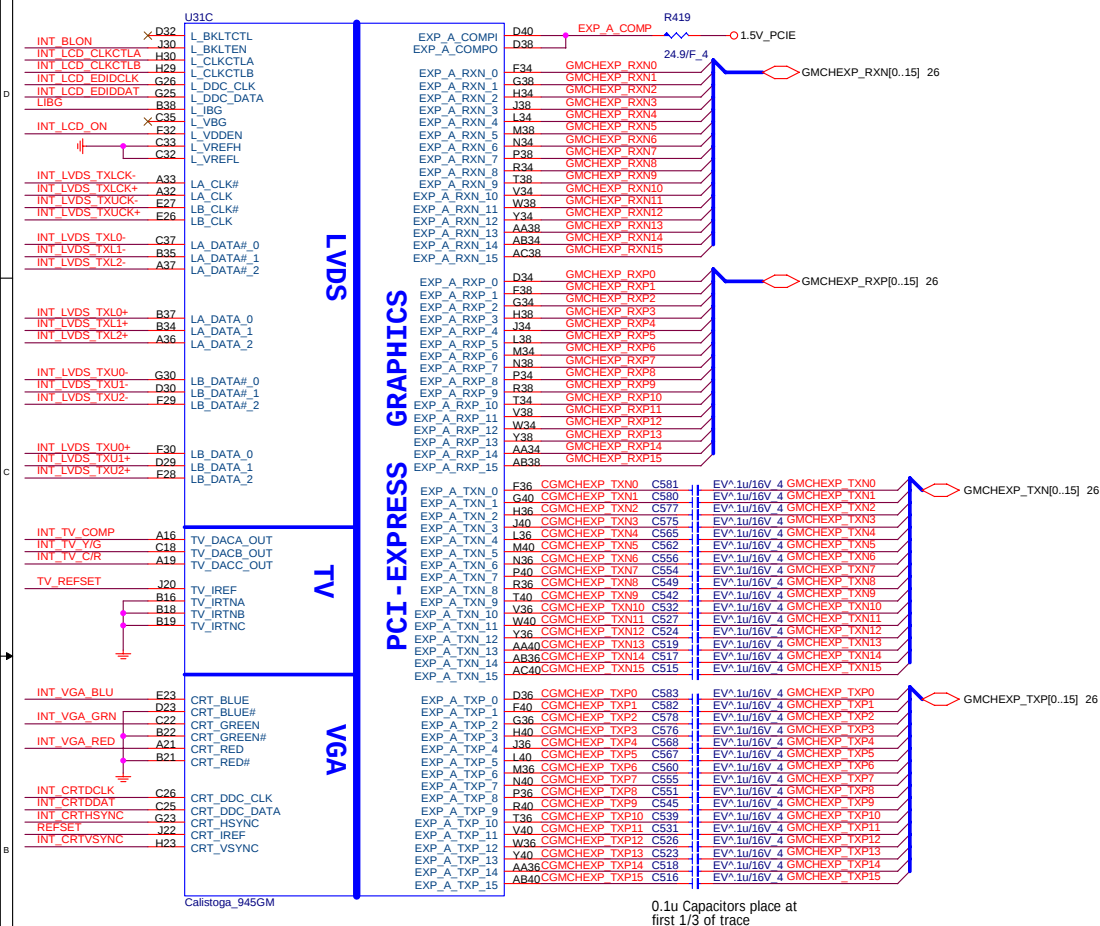
GMCH Strap pin



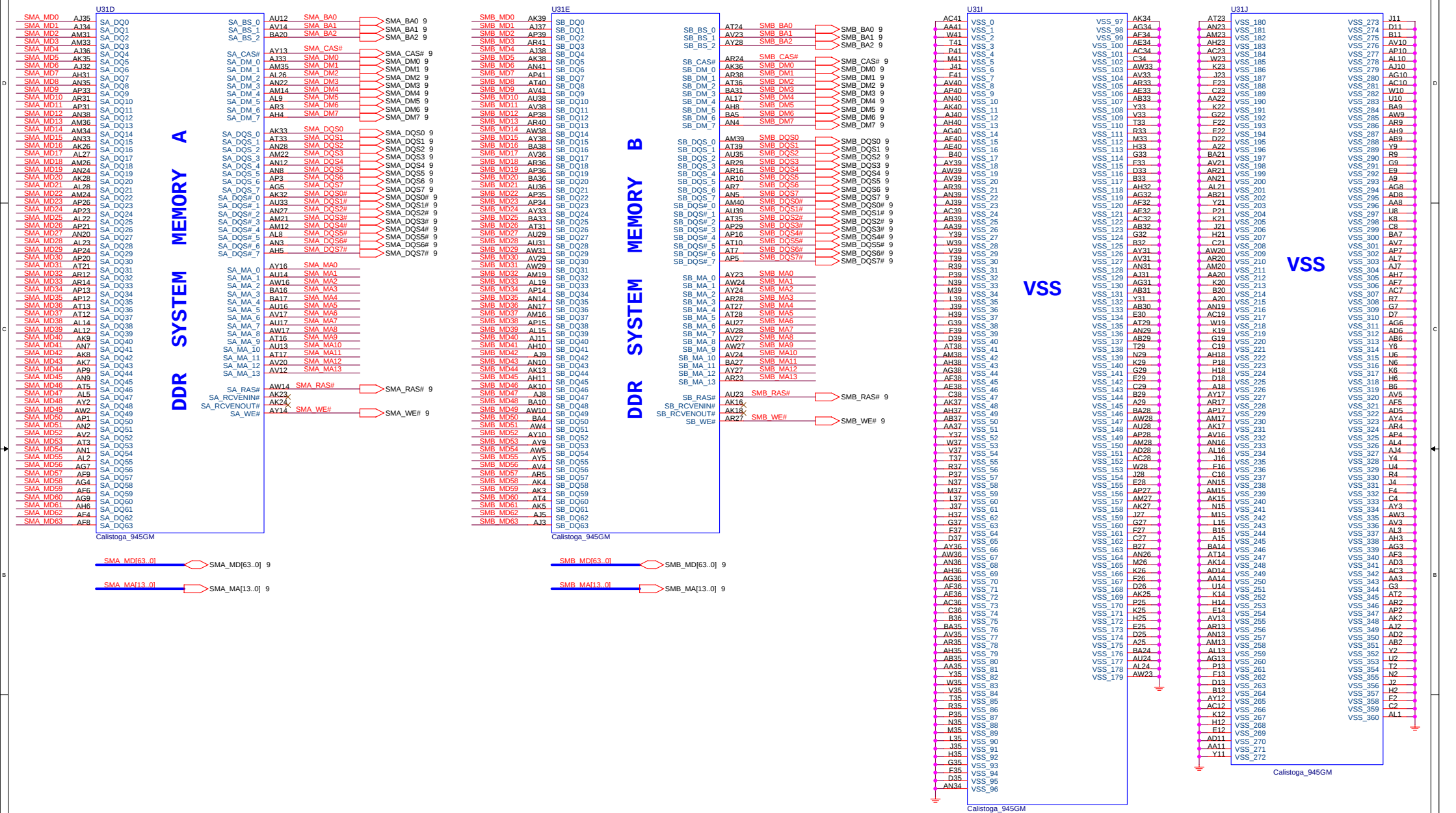
PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number GMCH (HOST / DMI)	Rev 1A
Date:	Wednesday, August 02, 2006	Sheet 5 of 30

DVO_CH7307

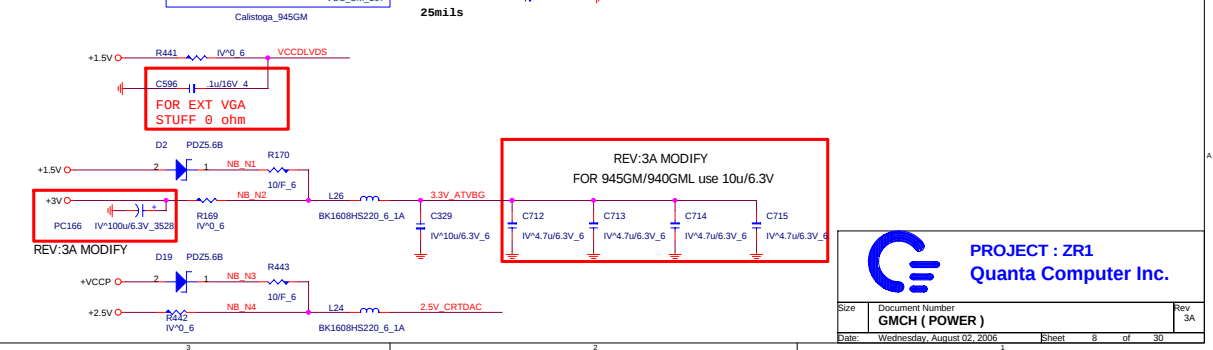
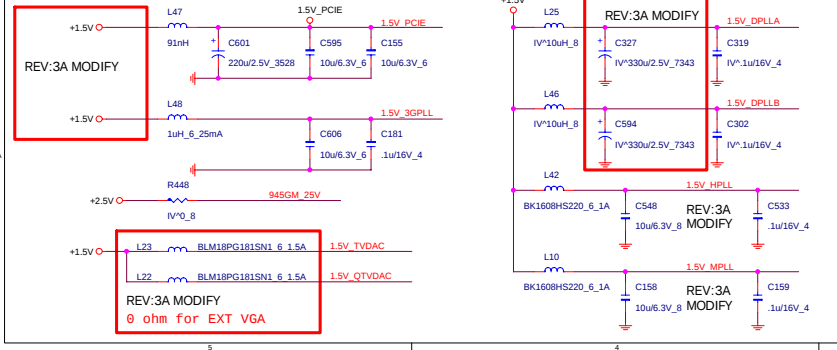
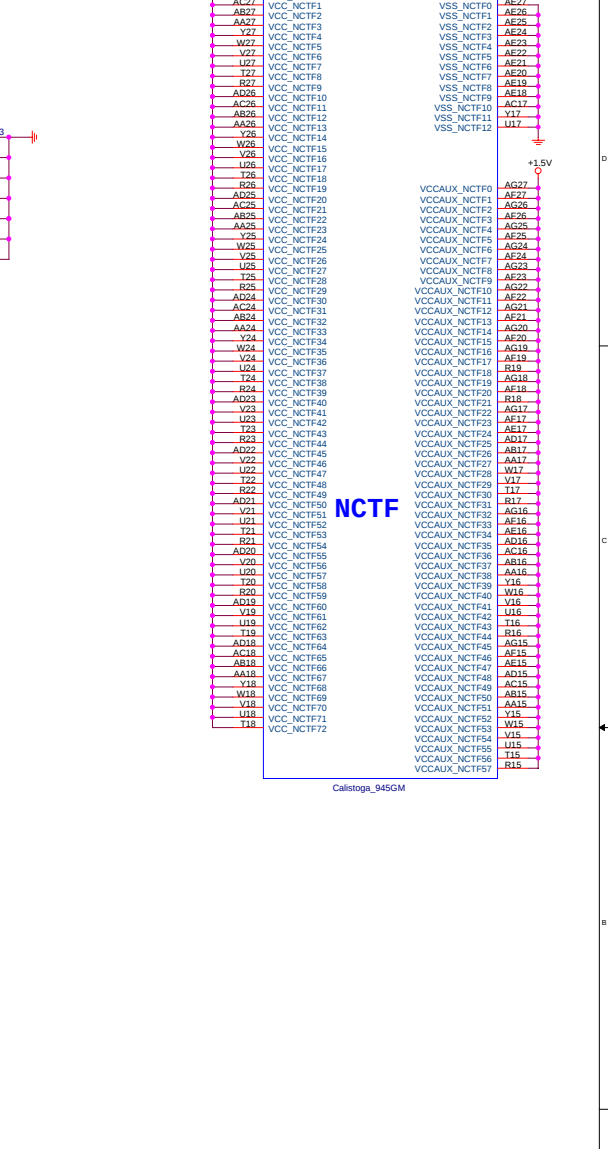
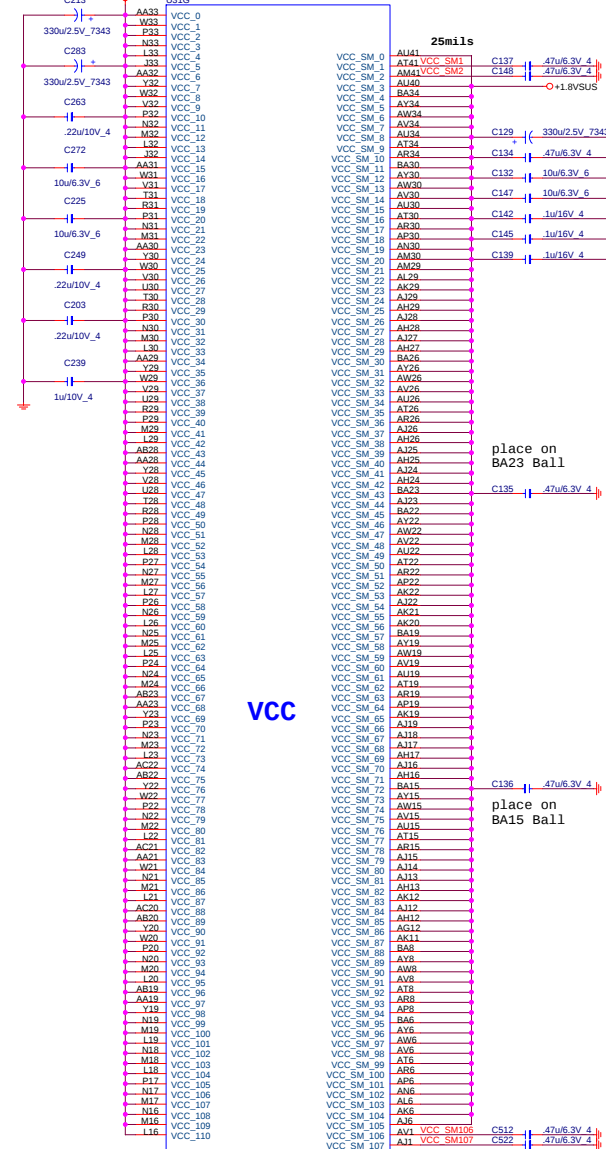
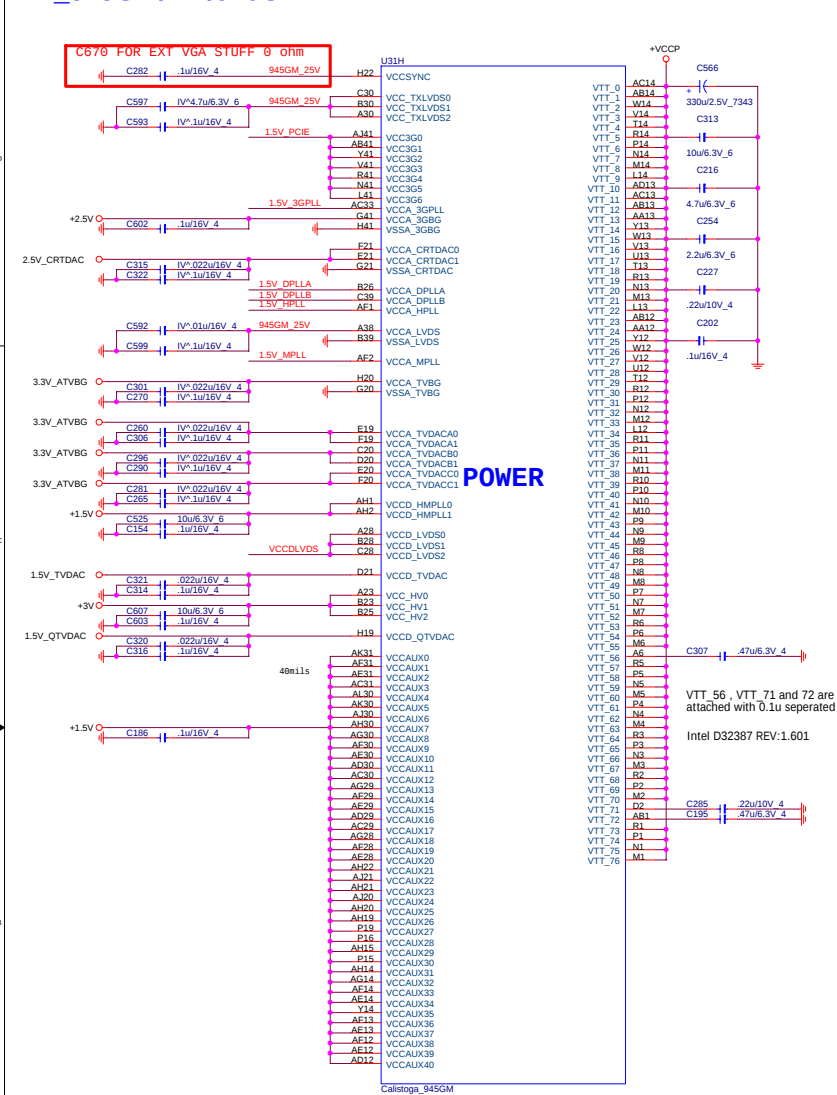


NB_945GM/PM/940GML



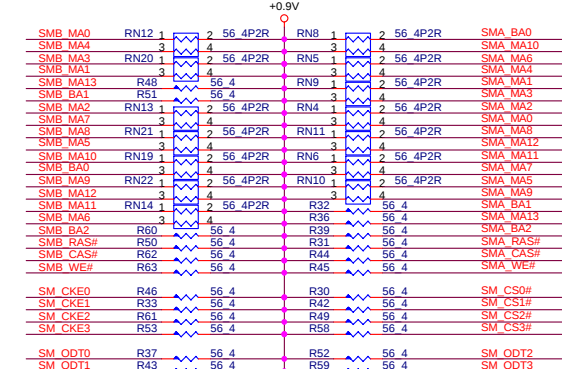
PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number GMCH (MEMORY)	Rev 1A
Date:	Wednesday, August 02, 2006	Sheet 7 of 30

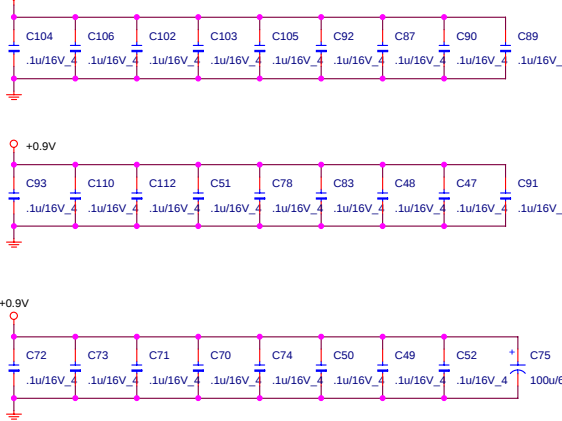
NB 945GM/PM/940GML

DDR2 SO-DIMM SOCKET

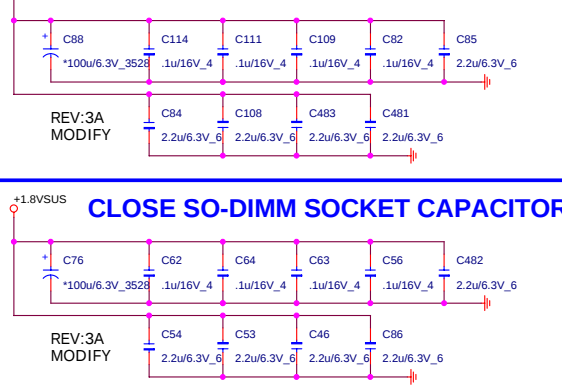
DDR2 TERMINATOR



TERMINATOR DECOUPLING CAPACITOR

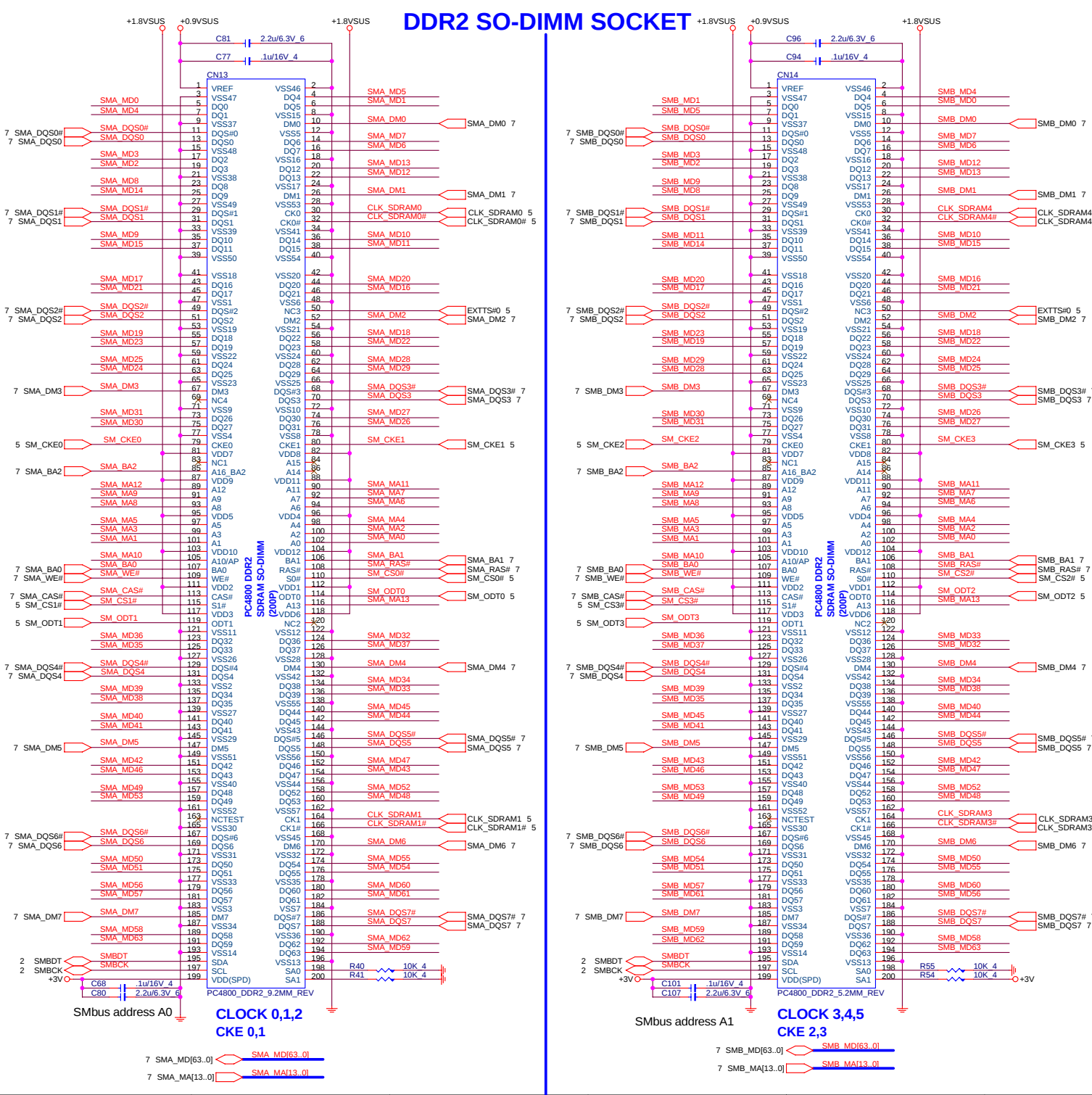


CLOSE SO-DIMM SOCKET CAPACITORS

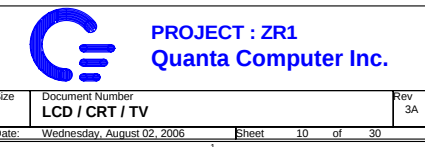
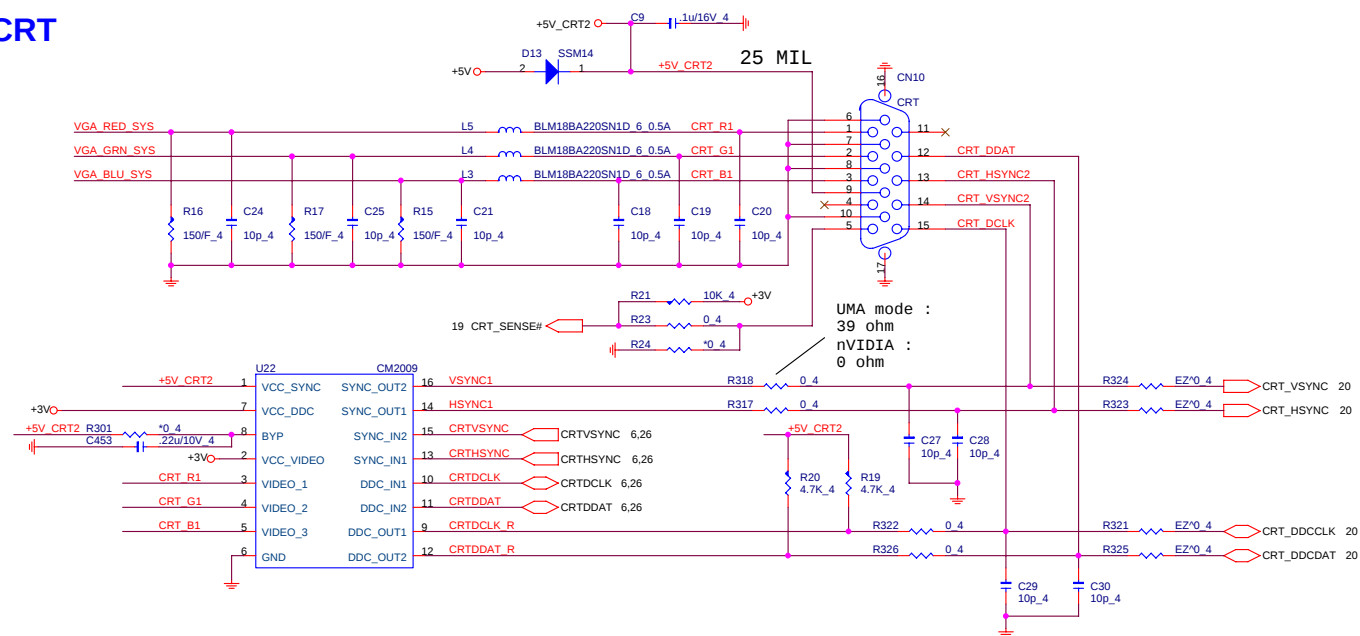
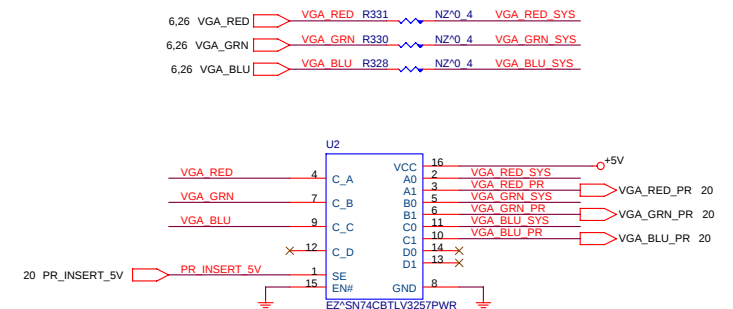


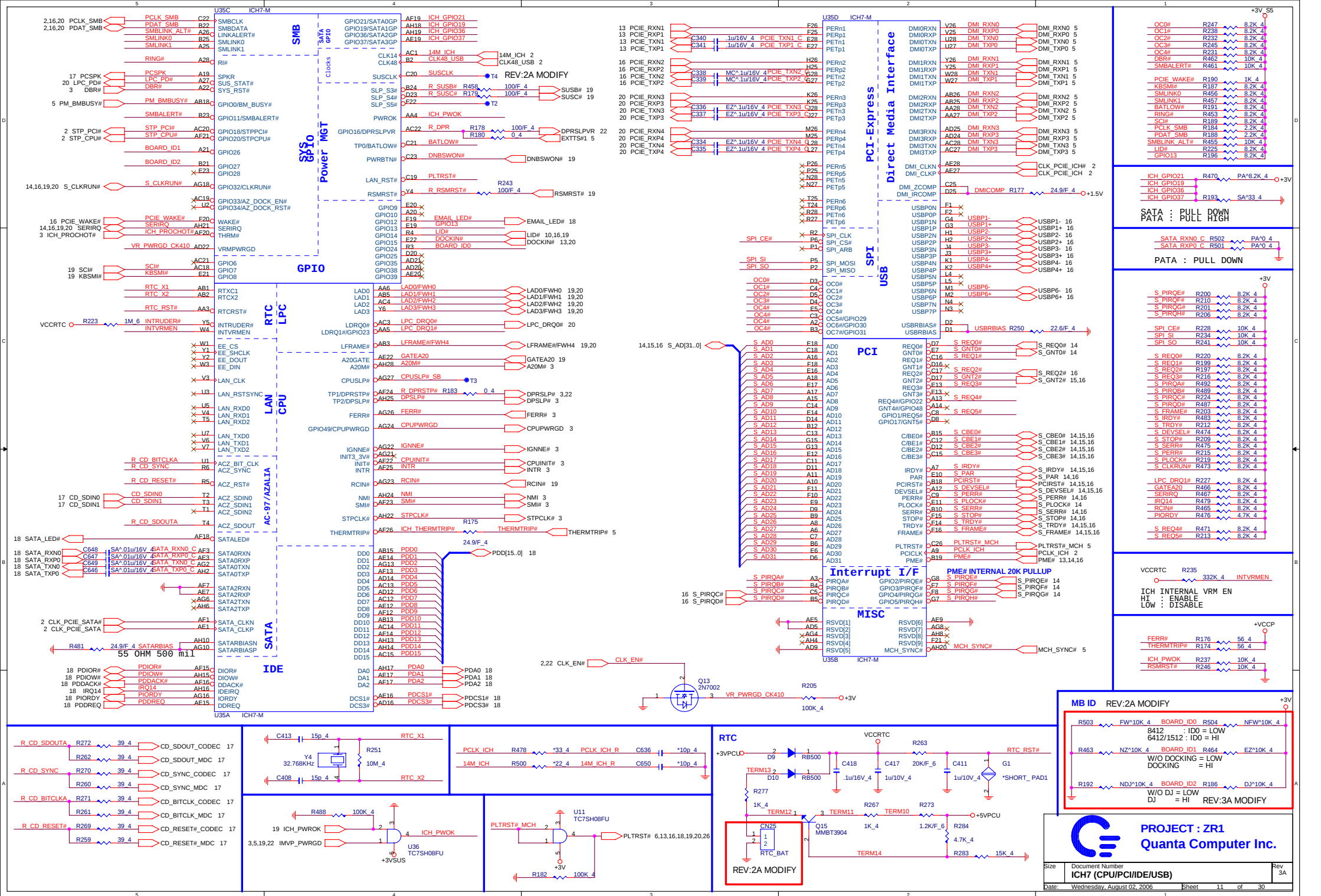
PROJECT : ZR1
Quanta Computer Inc.

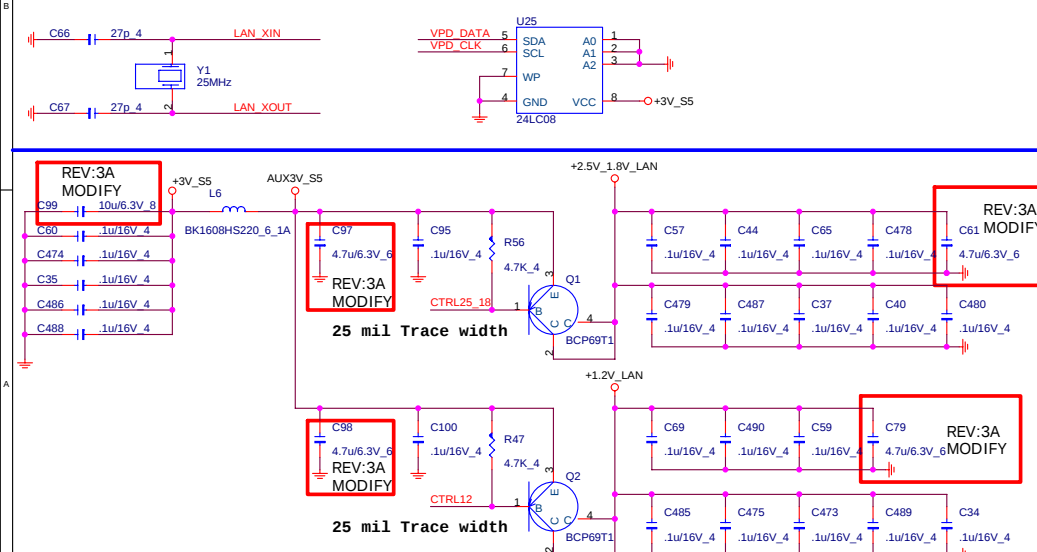
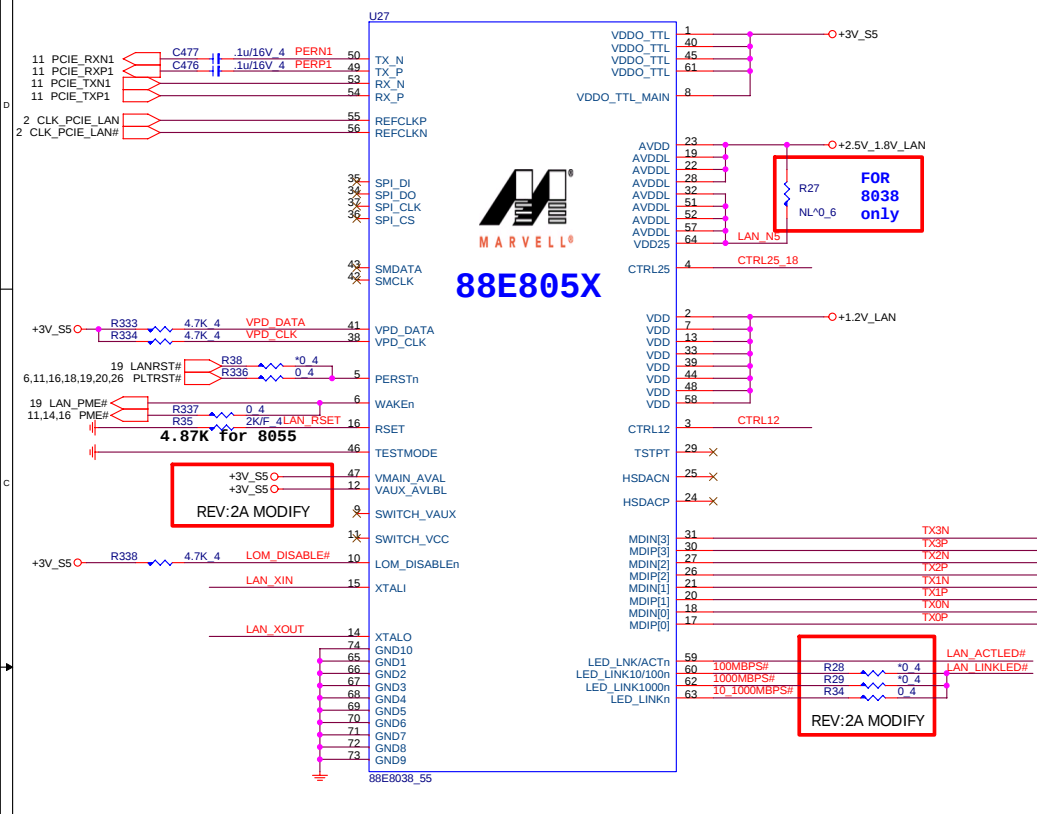
Size	Document Number	Rev
DDR SO-DIMM(200P)		3A
Date	Wednesday, August 02, 2006	Sheet 9 of 30



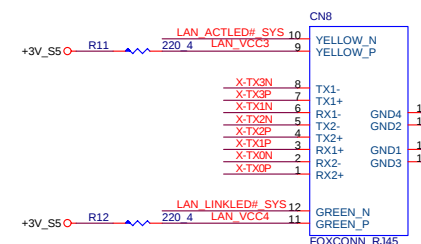
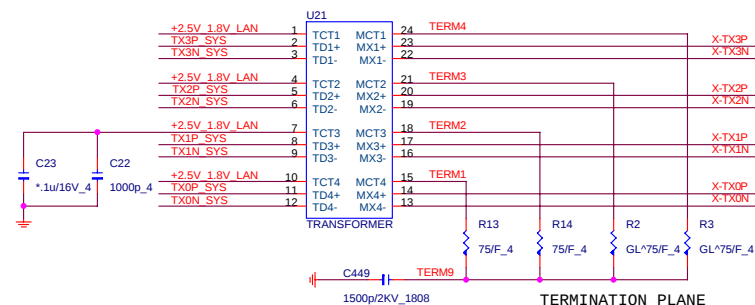
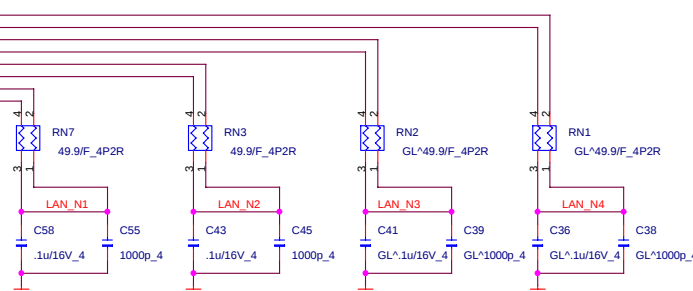
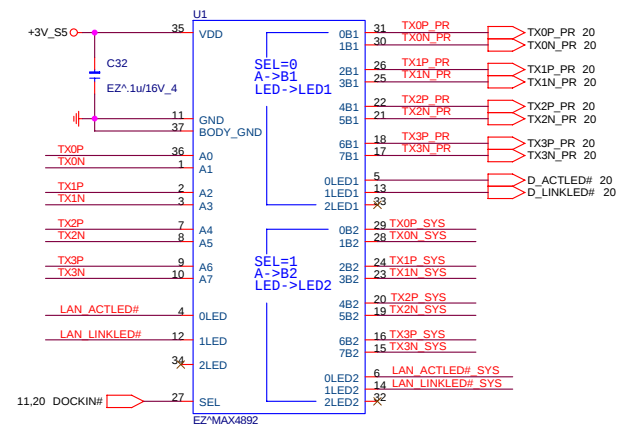
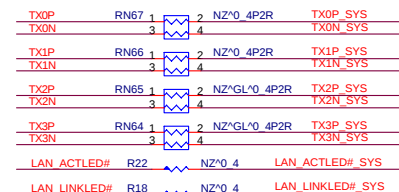
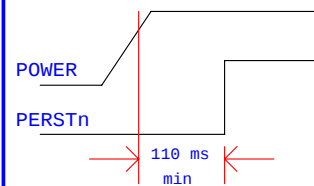
CRT





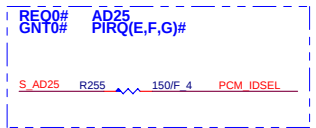


RESET TIMING

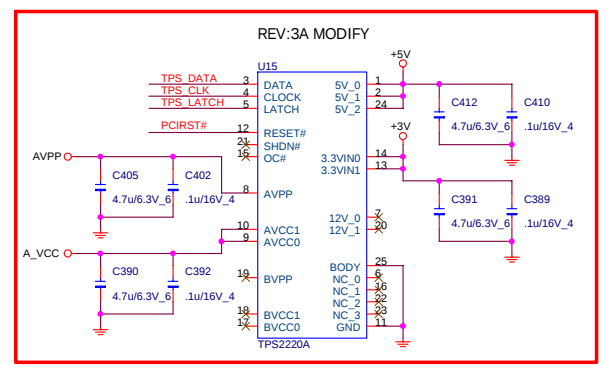
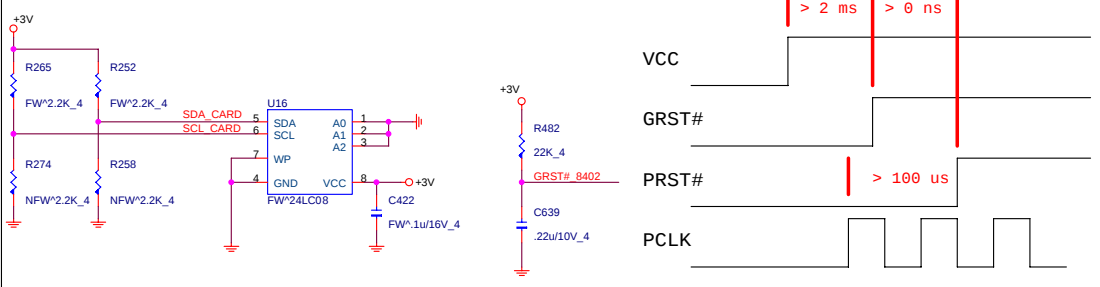
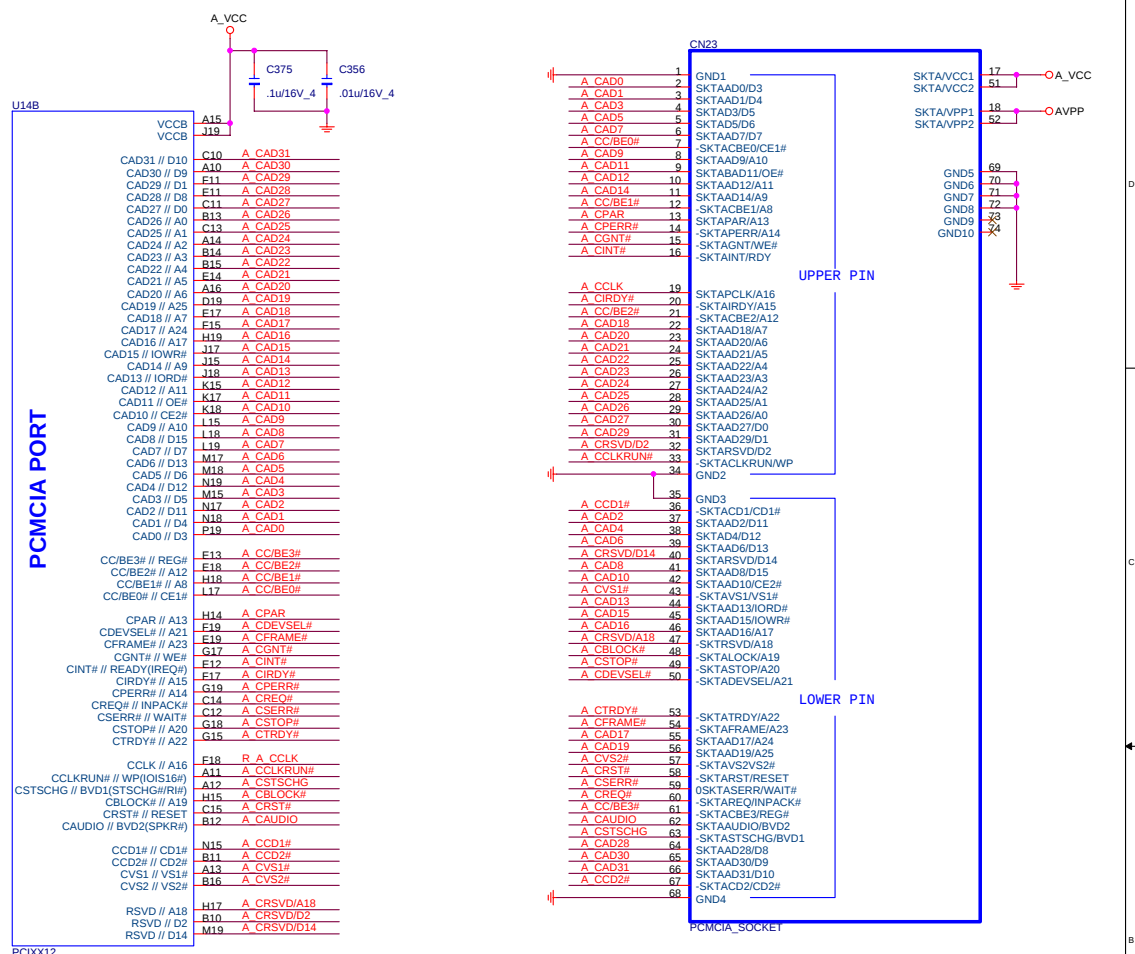
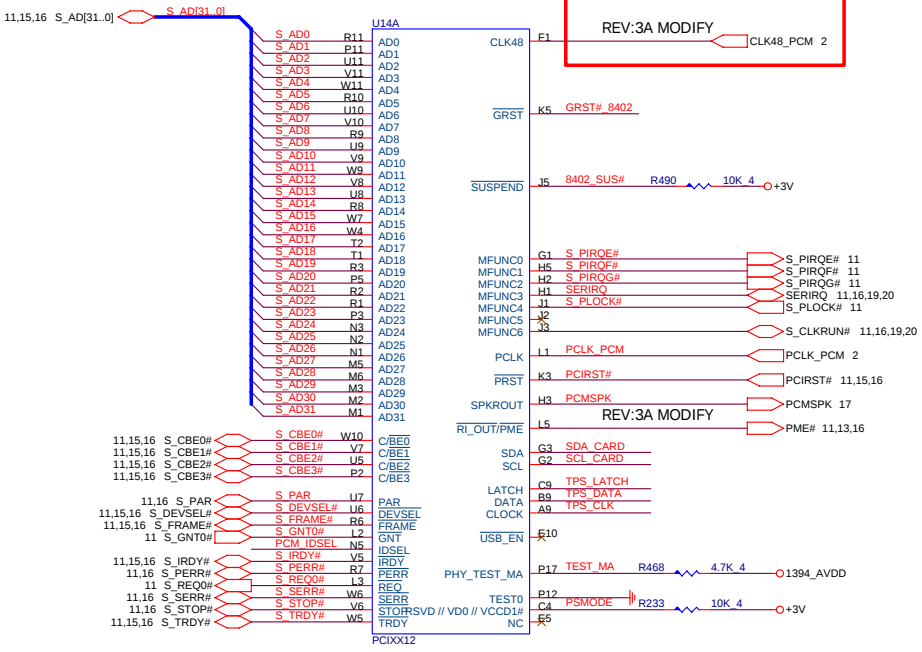


PROJECT : ZR1
Quanta Computer Inc.

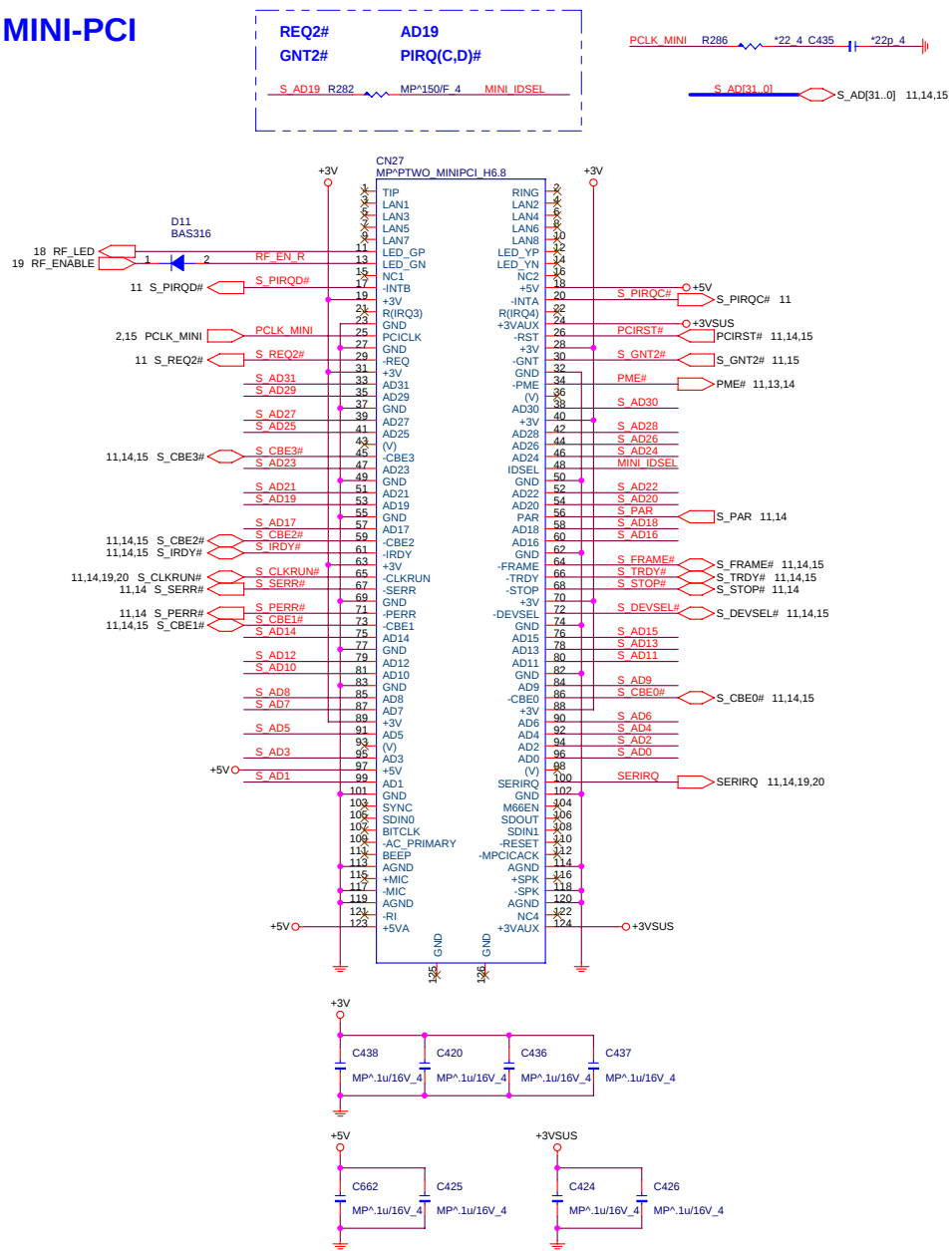
PCIXX12_PCMCIA



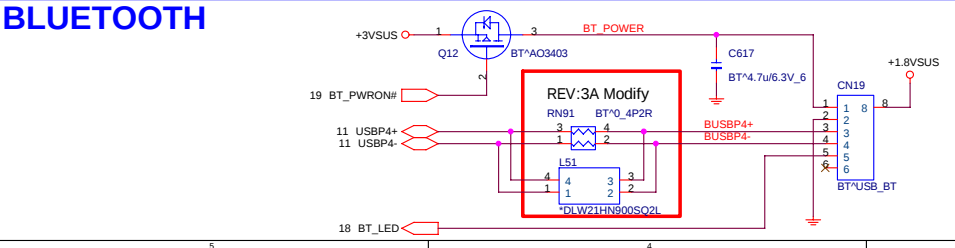
PCI8412 : AJ084120T08 PCMCIA / 1394 / 5 IN 1
PCI6412 : AL064120T04 PCMCIA / 5 IN 1



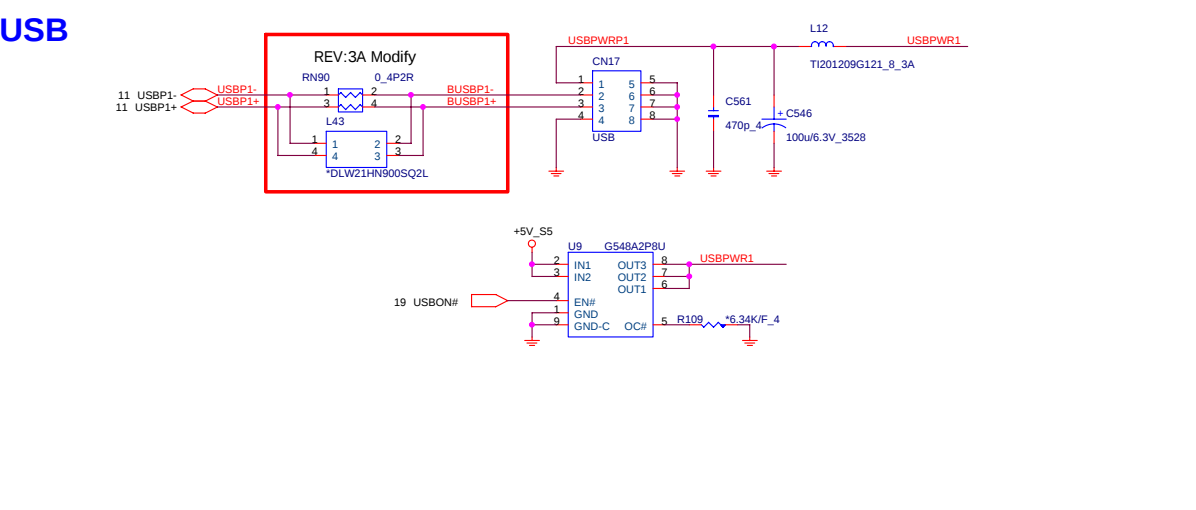
MINI-PCI



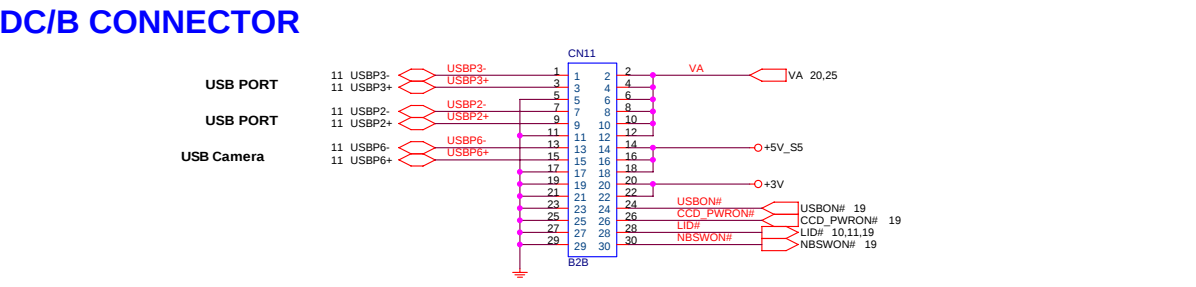
BLUETOOTH



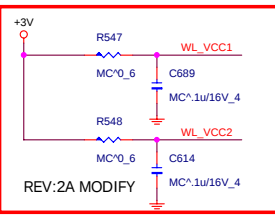
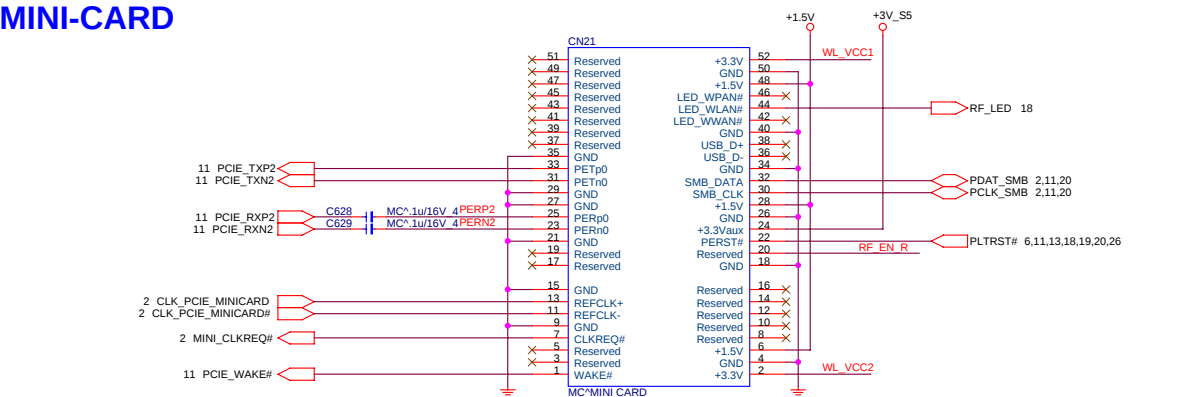
USB



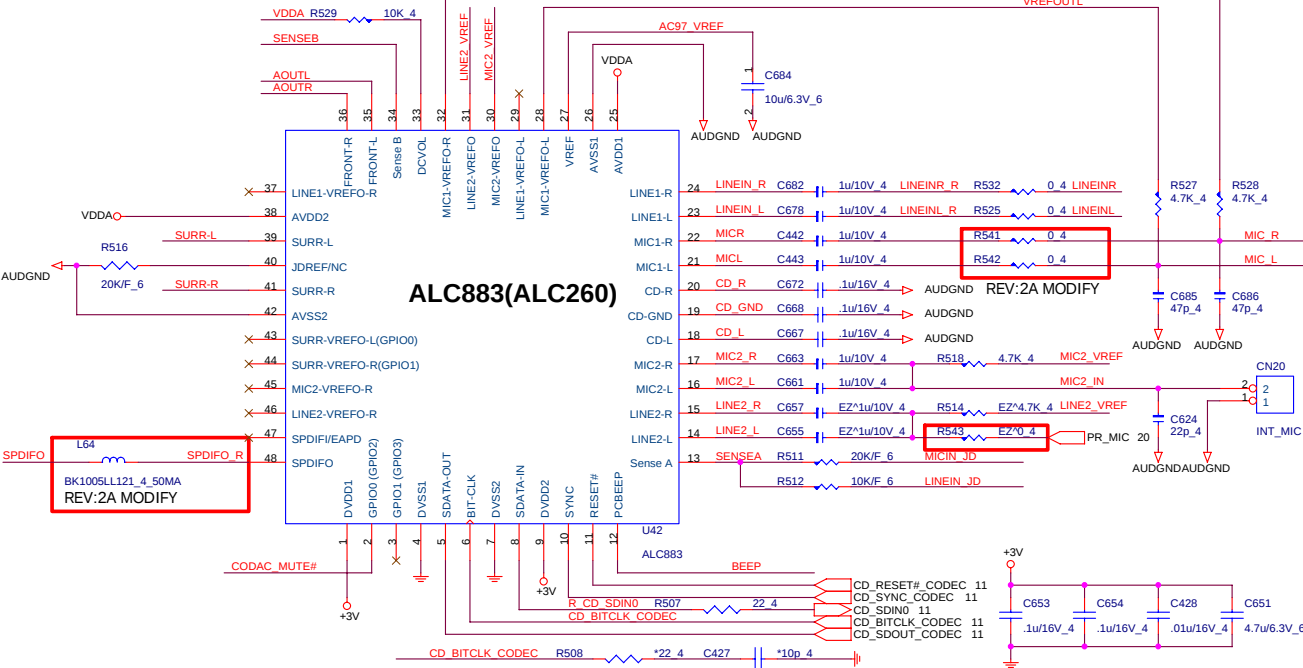
DC/B CONNECTOR



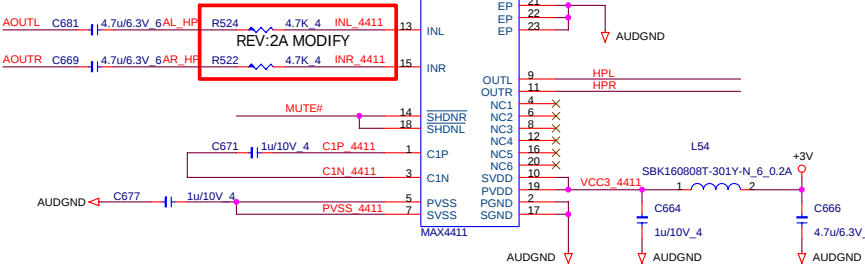
MINI-CARD



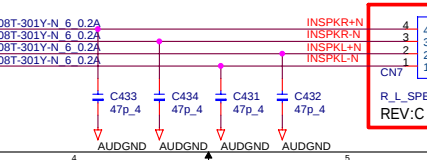
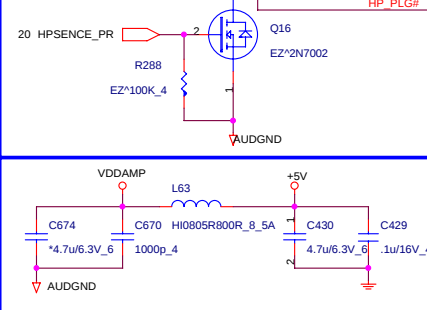
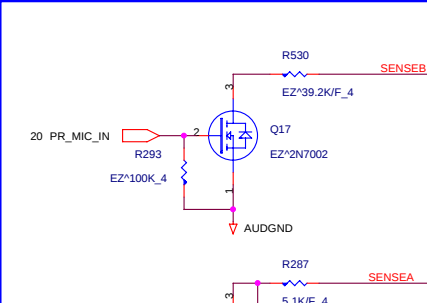
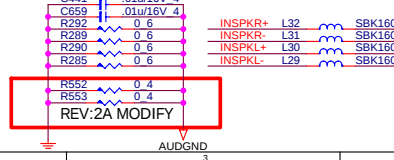
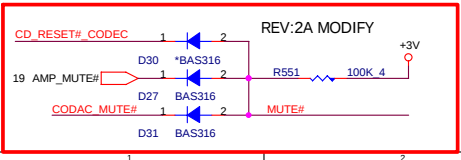
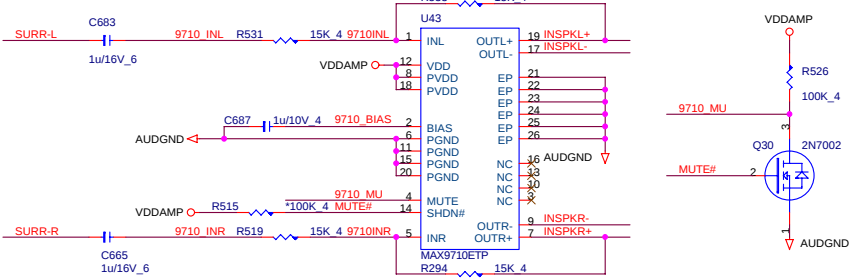
Audio Codec_ALC883



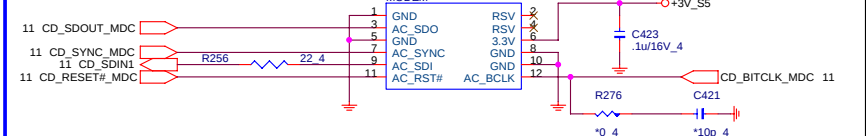
LINE OUT Amplifier



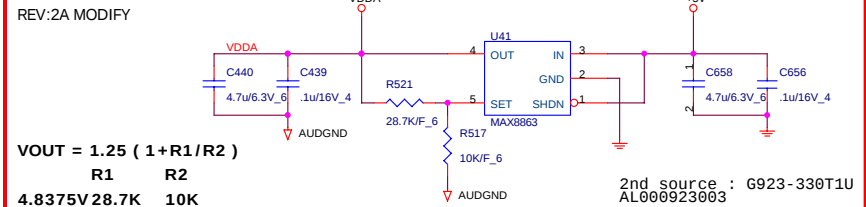
SPEAKER Amplifier



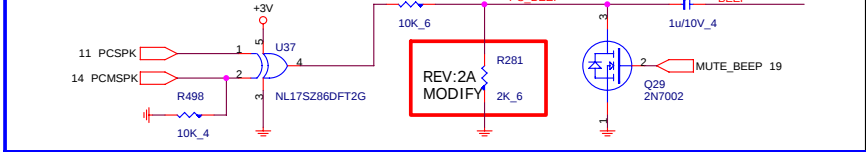
MDC



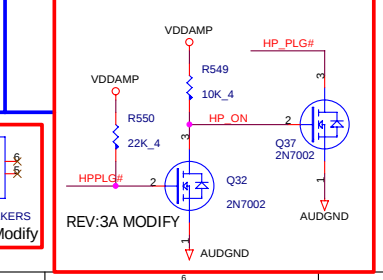
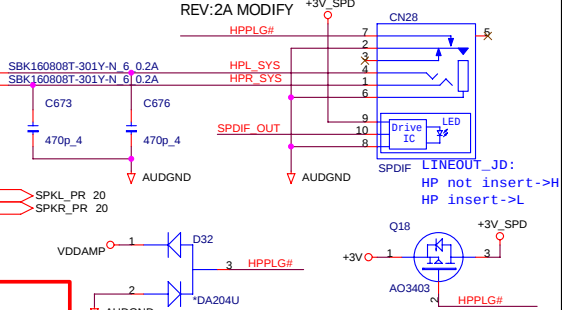
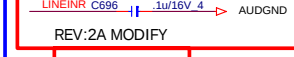
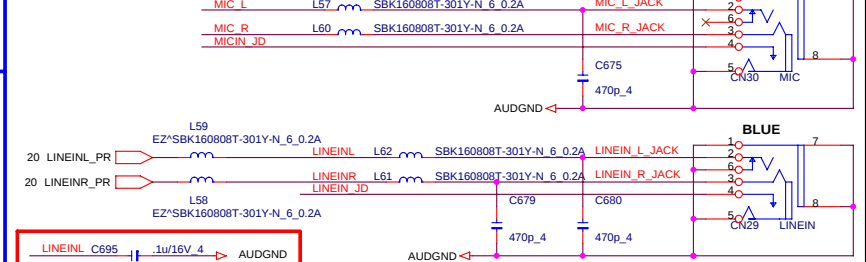
Audio Codec Power



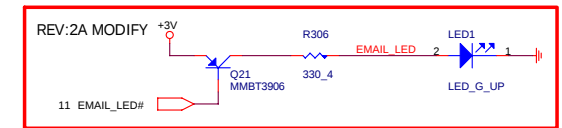
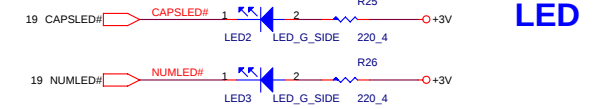
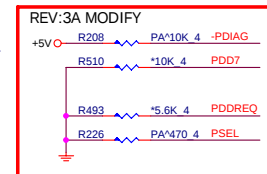
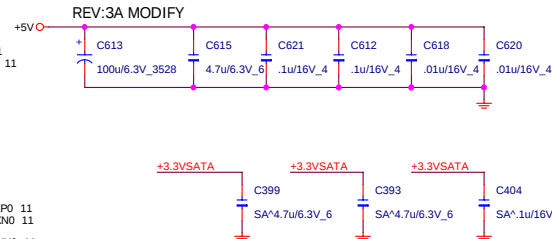
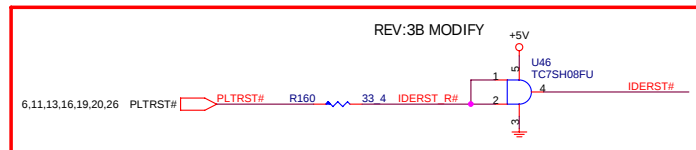
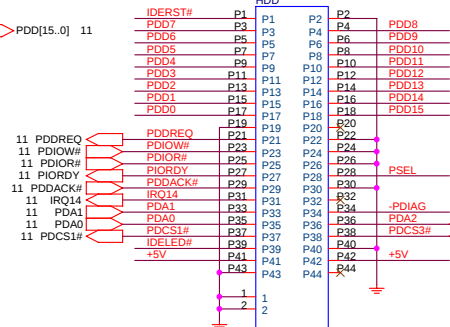
BEEP



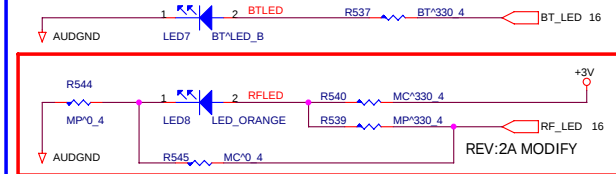
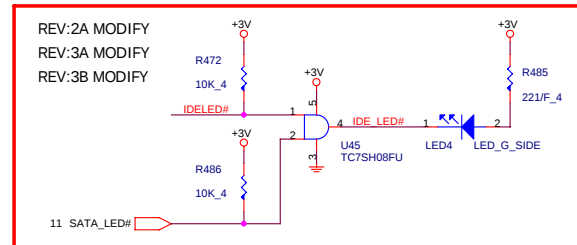
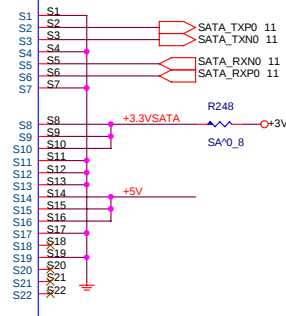
Audio Jack



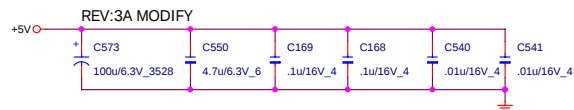
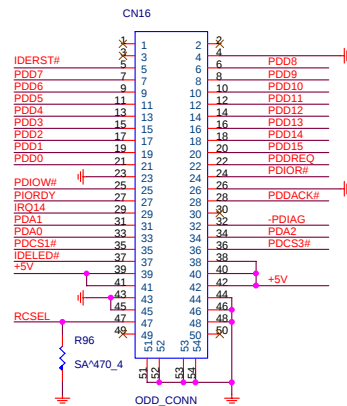
HDD



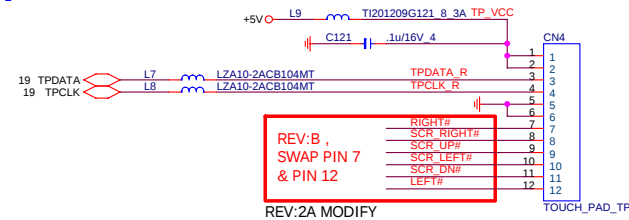
SATA



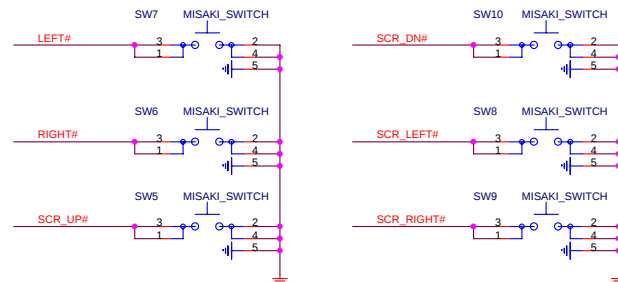
ODD



TP CONN



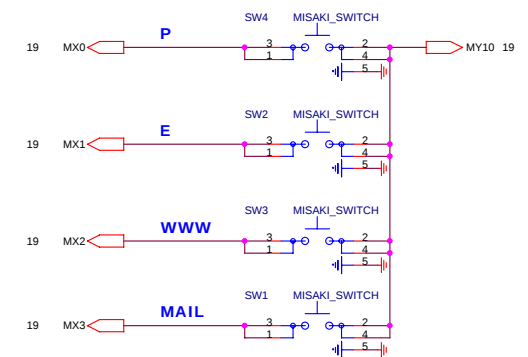
TP SWITCH



WL & BT SWITCH



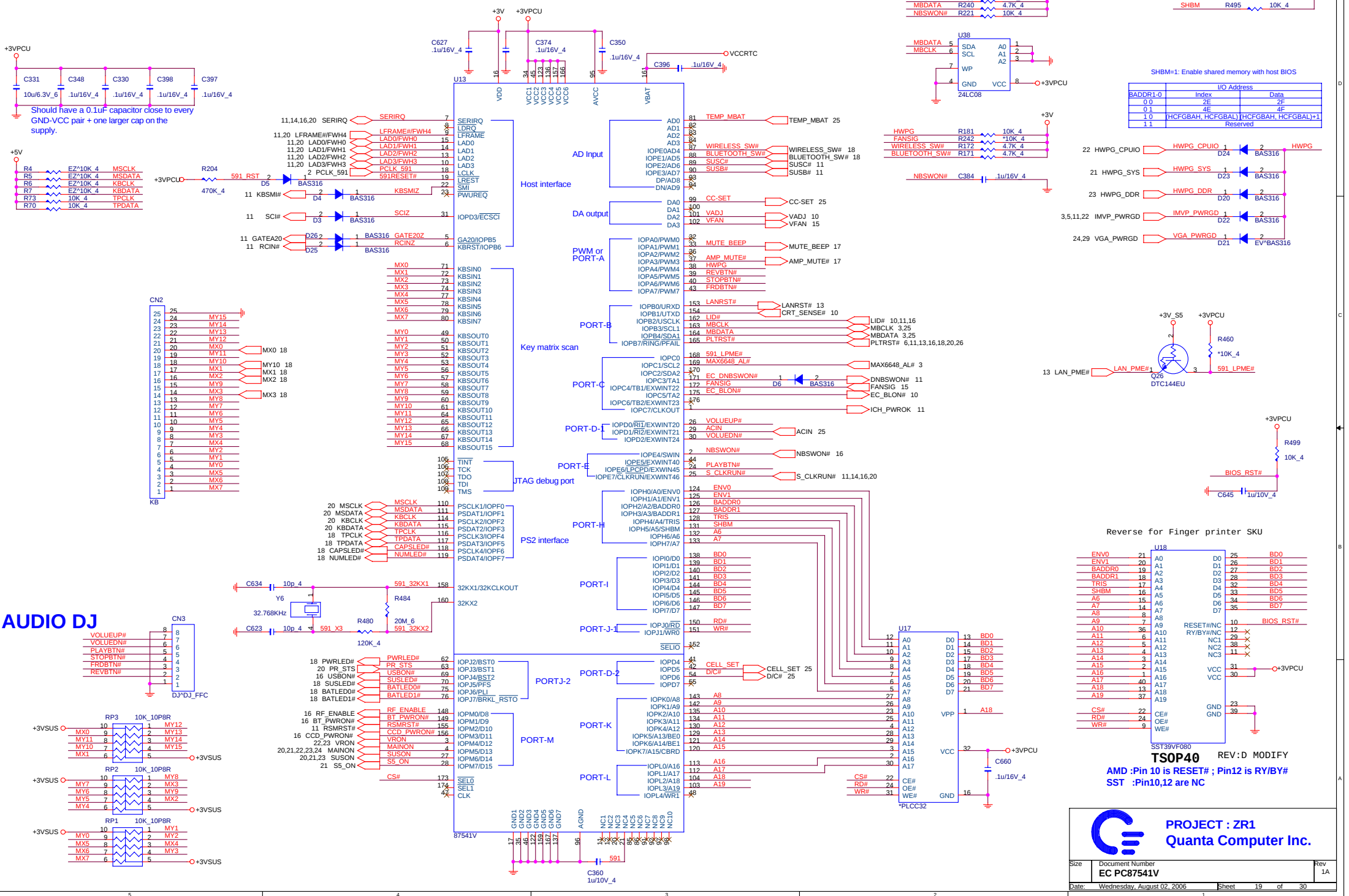
QUICK KEY SWITCH



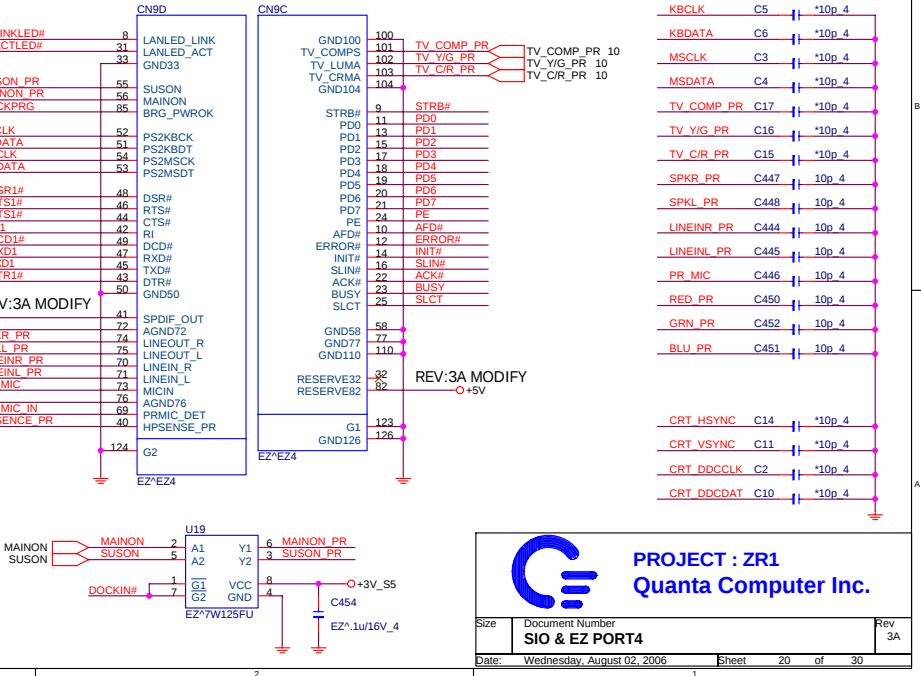
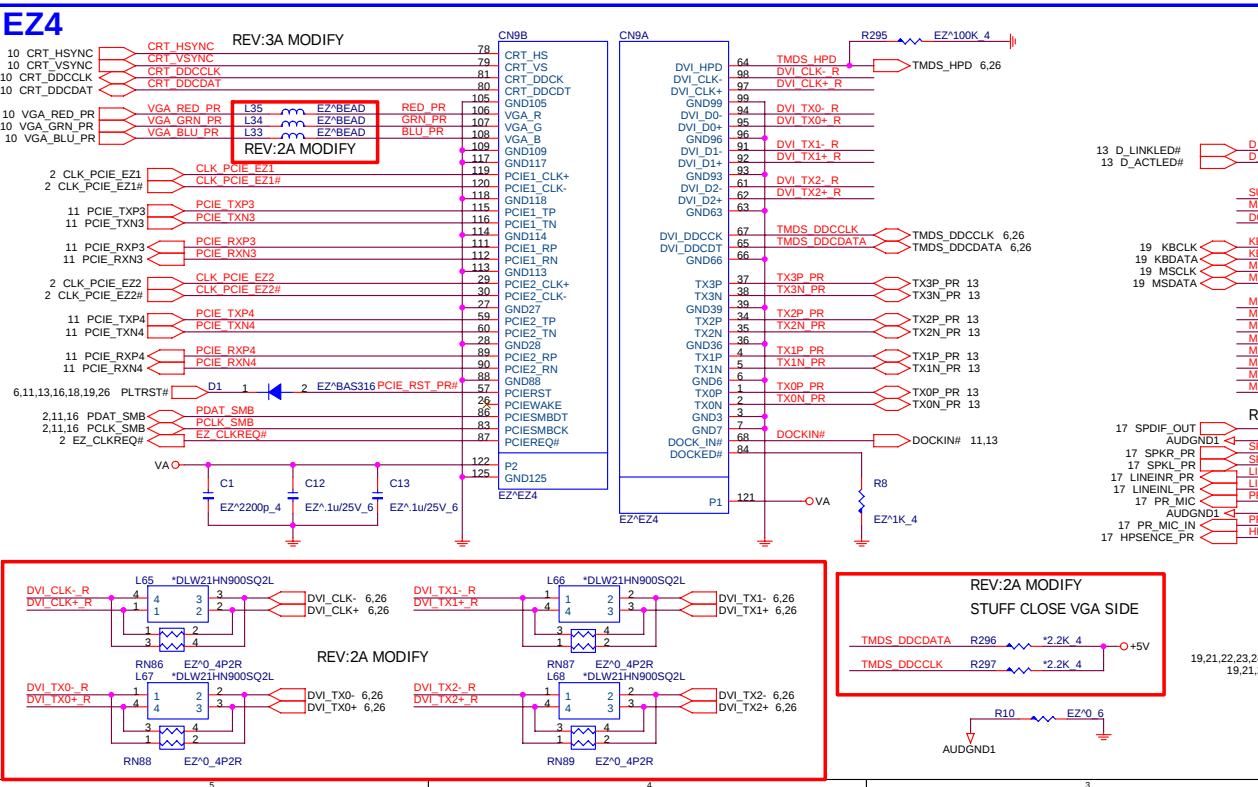
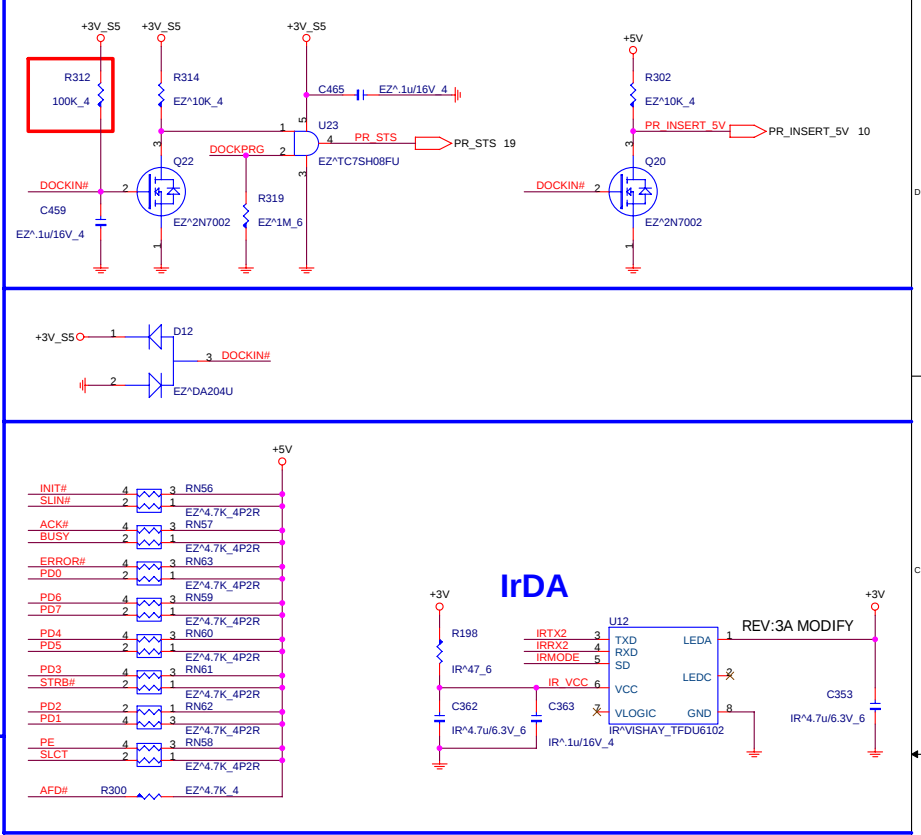
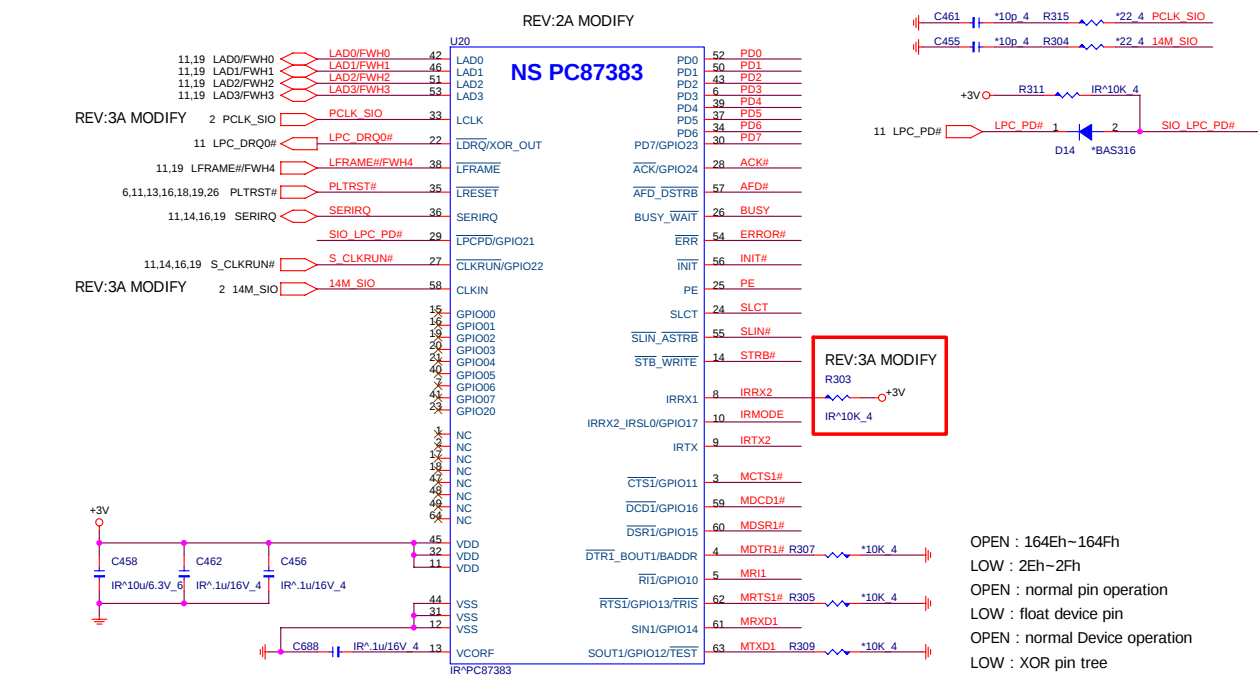
PROJECT : ZR1
Quanta Computer Inc.

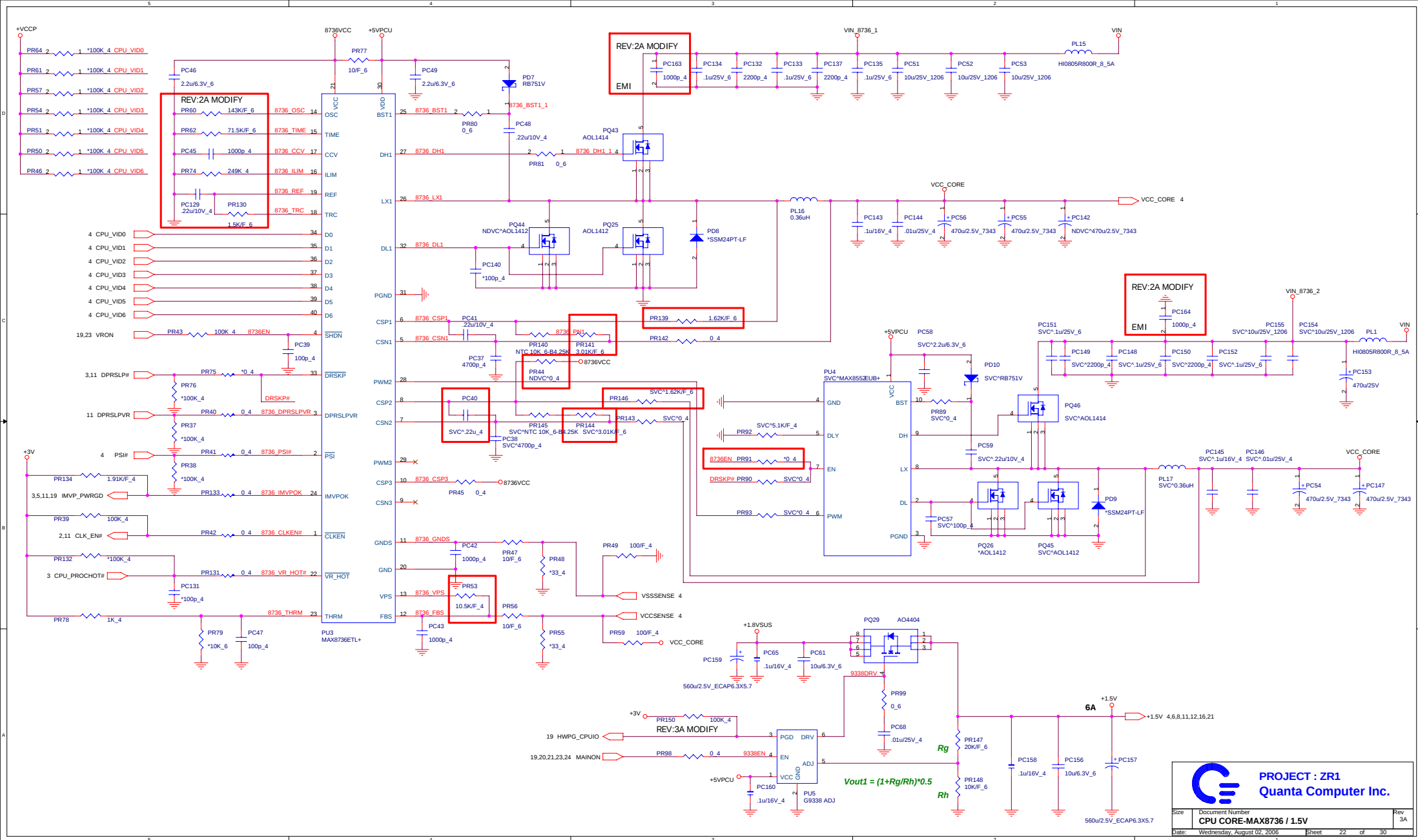
Size	Document Number HDD/ODD/LED/SW/TP	Rev 3A
Date:	Wednesday, August 02, 2006	Sheet 18 of 30

K/B CONTROLLER

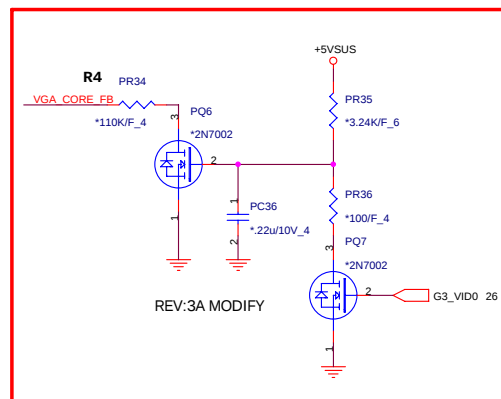
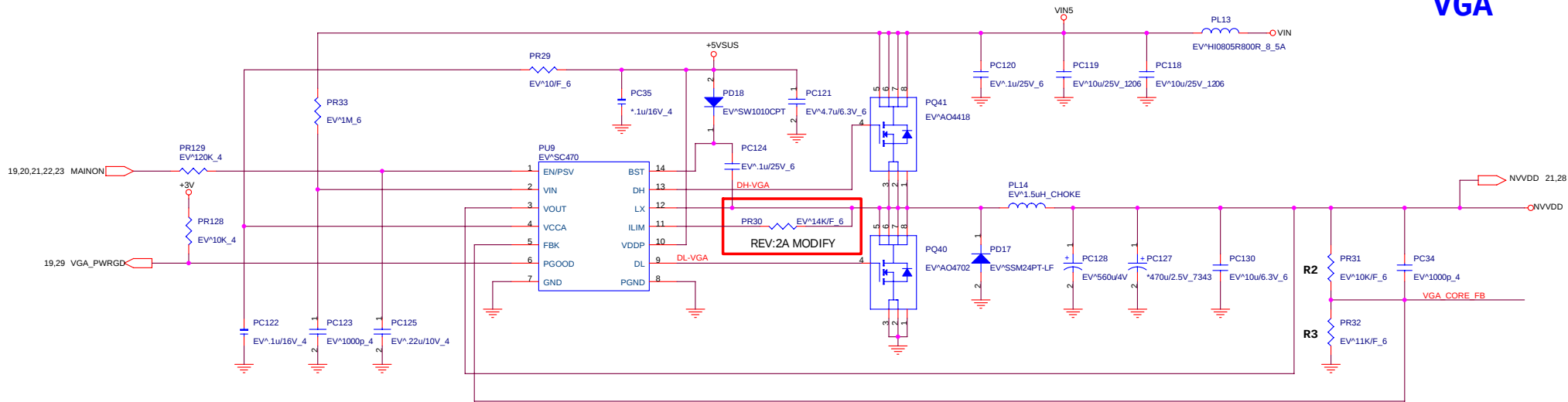


NS SIO 87383





VGA



$$HI \rightarrow V_{OUT} = (1 + R_2/R_3) * 0.5$$

L0 - -> $V_{OUT} = (1 + R_2 / (R_3 // R_4)) * 0.5$

M52P (G)

PR1 : 10K

PR4 : 11K
PR2 : 110K

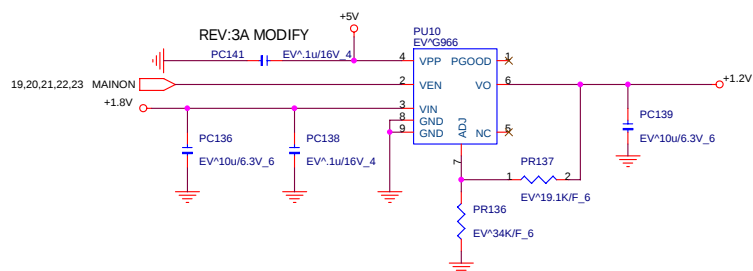
M54P

PR1 : 12K

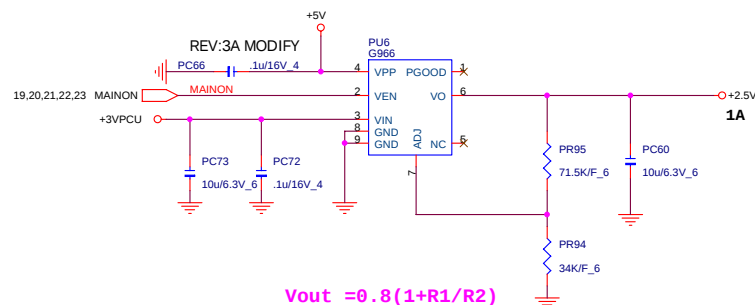
PR4 : 12K
PR2 : 60.4K

Power Play Mode

VGA_PWR_SW		VGA_CORE
	HI	0.95V--M52P(G) 1.0V --M54P
Default	LO	1.0V--M52P(G) 1.1V--M54P



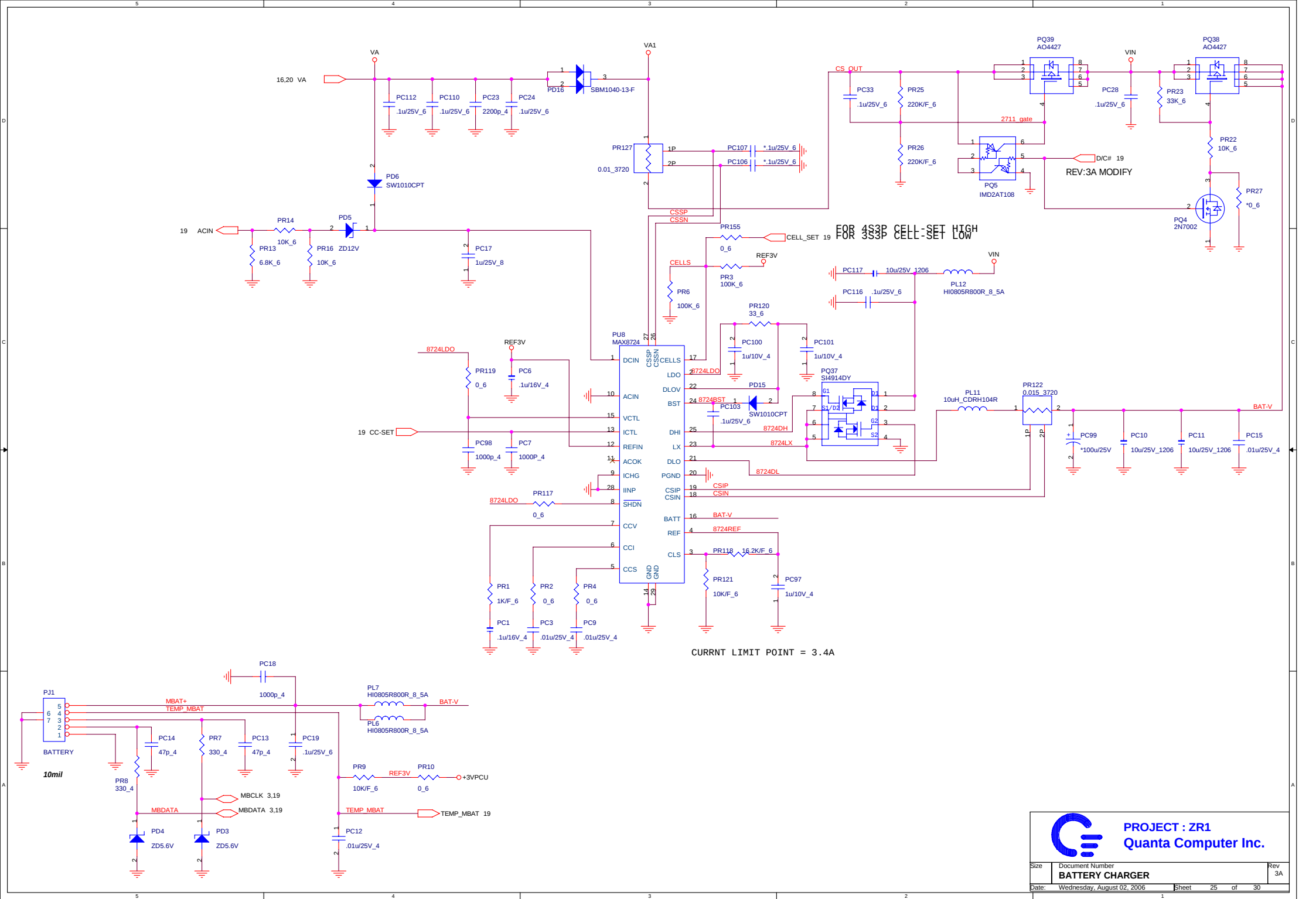
$$V_{out} = 0.8(1 + R_1/R_2) = 0.8(1 + 20K/20K) = 1.2V$$



$$\begin{aligned} V_{out} &= 0.8(1 + R_1/R_2) \\ &= 0.8(1 + 20K/20K) = \\ &2.5V \end{aligned}$$



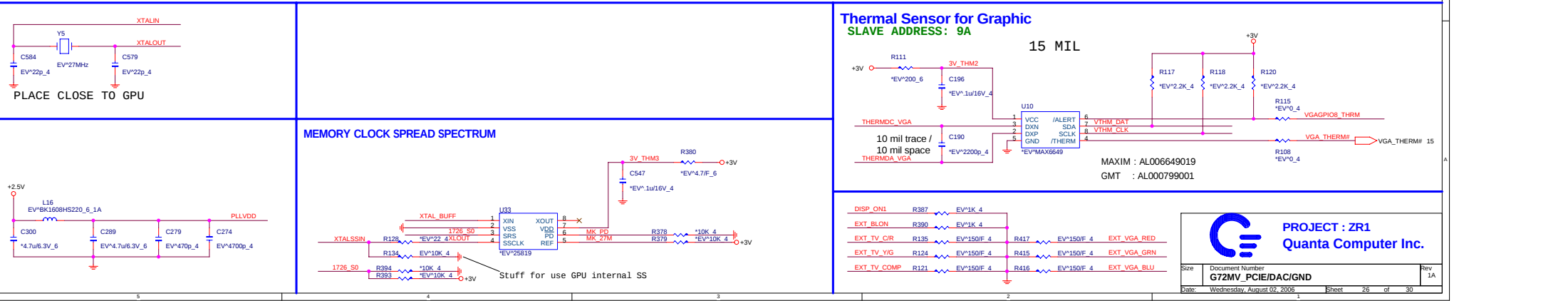
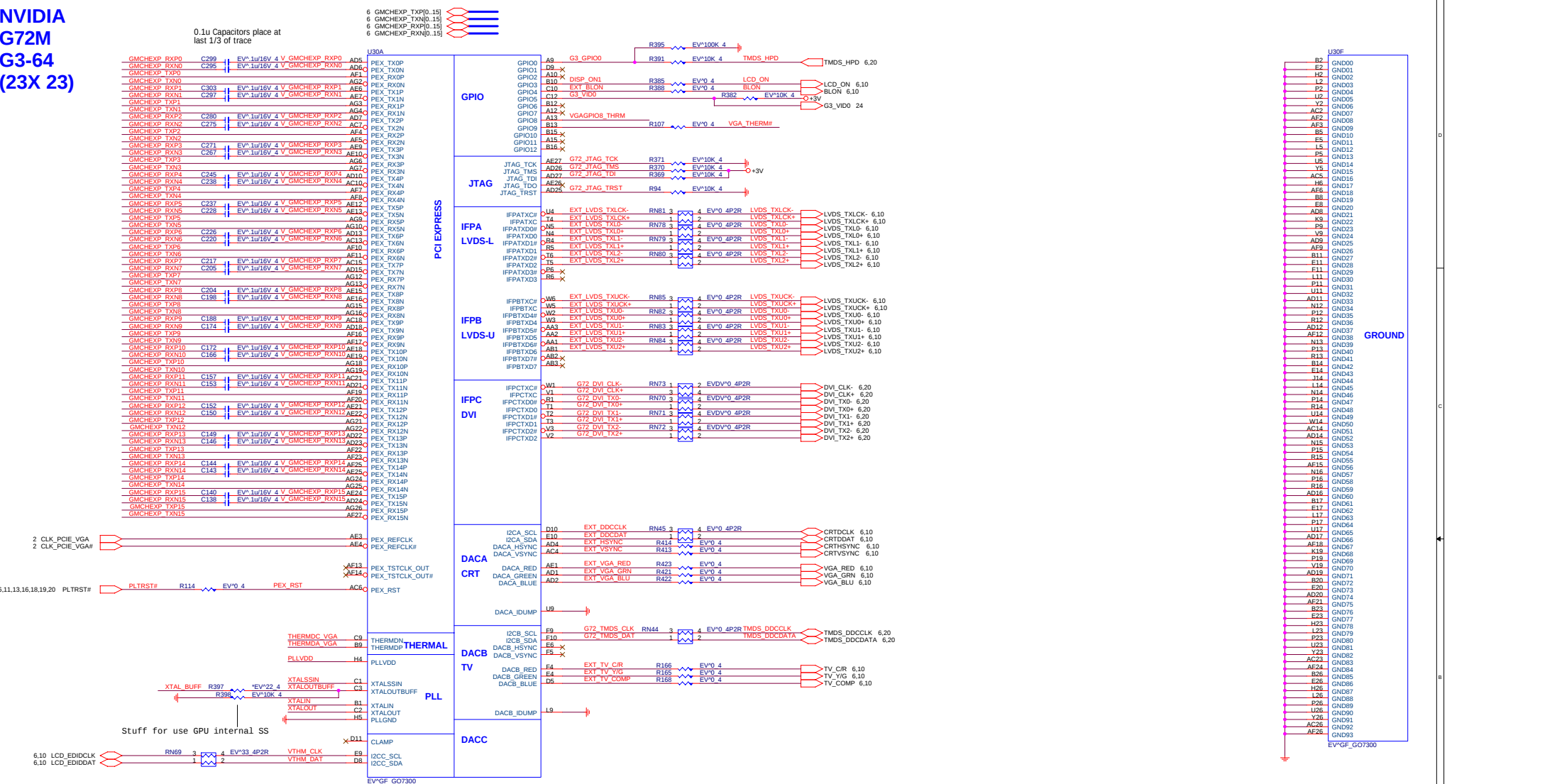
PROJECT : ZR1
Quanta Computer Inc.

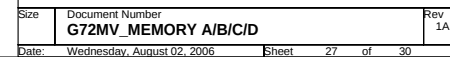


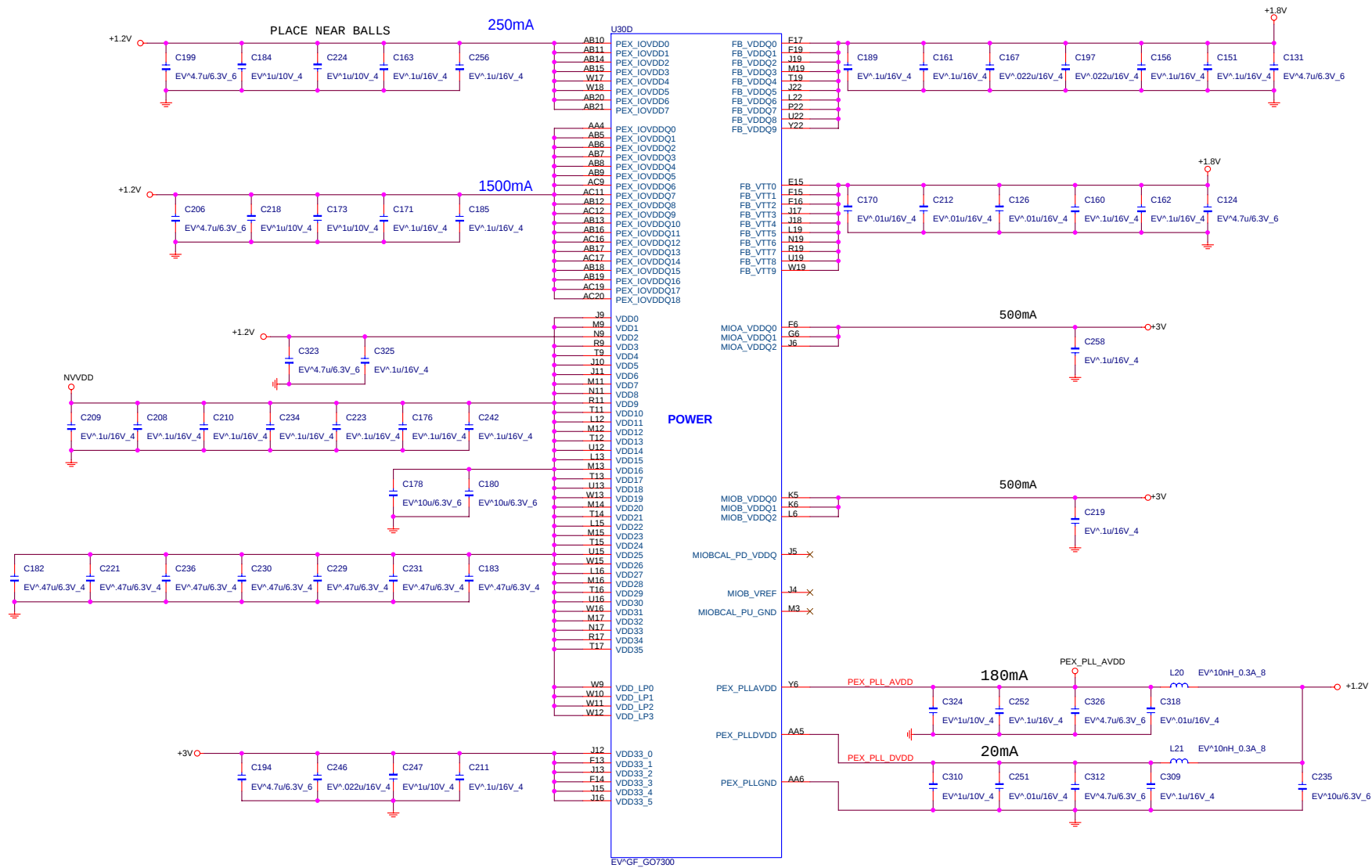
PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number	Rev
	BATTERY CHARGER	3A
Date:	Wednesday, August 02, 2006	Sheet 25 of 30

NVIDIA
G72M
G3-64
(23X 23)

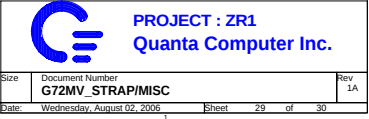






PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number	Rev
	G72MV_POWER	1A
Date:	Wednesday, August 02, 2006	Sheet 28 of 30



www.s-manuals.com